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## **OPTICAL INTERCONNECTS FOR HIGH SPEED COMPUTING**

**Franz Haas, Paul R. Cook and John E. Malowicki**

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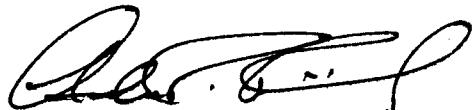
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## **Abstract**

A novel optical interconnect scheme for multichip module-to-multichip module interconnects has been developed which overcomes the traditional limitations of this technology, alignment complexity and implementation cost. Densely packed optical channels are guided by fiber optic plate material embedded into the modules. System alignment is simplified by alleviating the need to align a complex optical system, and by facilitating the alignment of one multichip module with another. No expensive micro lens (diffractive, refractive or holographic) technology is required. This technology will greatly increase the number and speed of data interconnects between multichip modules while reducing the space requirements for the interconnect system. These advances can provide faster computer systems in smaller packages, ideal advantages for aircraft, satellite, missile, and unmanned aerial vehicle (UAV) platforms.

## **1. Introduction:**

This report addresses the fundamental limitation of electronic methods of transmitting high speed information between analog or digital electronic circuits. The unique requirements of military air and space-based systems to occupy small volumes, to minimize power consumption, and to perform vast amounts of processing at high speeds demands that promising packaging technologies be explored to address these issues.

A novel optical interconnect scheme was designed based on integrating optically guiding material into the structure of the computer system<sup>1,2</sup>. The optically guiding material can channel thousands of densely spaced optical beams between computer boards, in this case, multichip modules. By incorporating the 'optical system' into the module itself the alignment complexity and cost is greatly reduced as compared to all other optical interconnect schemes. No costly micro optical devices such as diffractive optics, refractive micro-lenses, or holographic optical elements are required.

A 32-channel module-to-module optical interconnect demonstration was proposed to validate this architecture. Each channel would operate at 500MHz and be placed on 125µm centers. This scheme can be scaled to much larger number of interconnects operating at over 1GHz per channel. This report details the proposed interconnect scheme and the development of emitter and detector arrays designed for the demonstration. Also reported is the establishment of a wafer bonding facility to bond silicon to fiber optic plate wafers to produce highly efficient and functional photodetectors and to provide an extremely high interconnect density for chip-scale packaging.

All device fabrication was conducted by the authors at the Cornell Nanofabrication Facility. Device integration and testing was conducted at the Air Force Research Laboratory, Rome Research Site Photonic Center.

Unfortunately, this effort was terminated before the demonstration could be completed. Two patents were awarded for the designs developed under this effort, United States Patent #5,652,811, "Semiconductor on Fiber Optic Substrate (SOFOS)" and United States Patent #5,848,214, "Optically-Guiding Multichip Module".

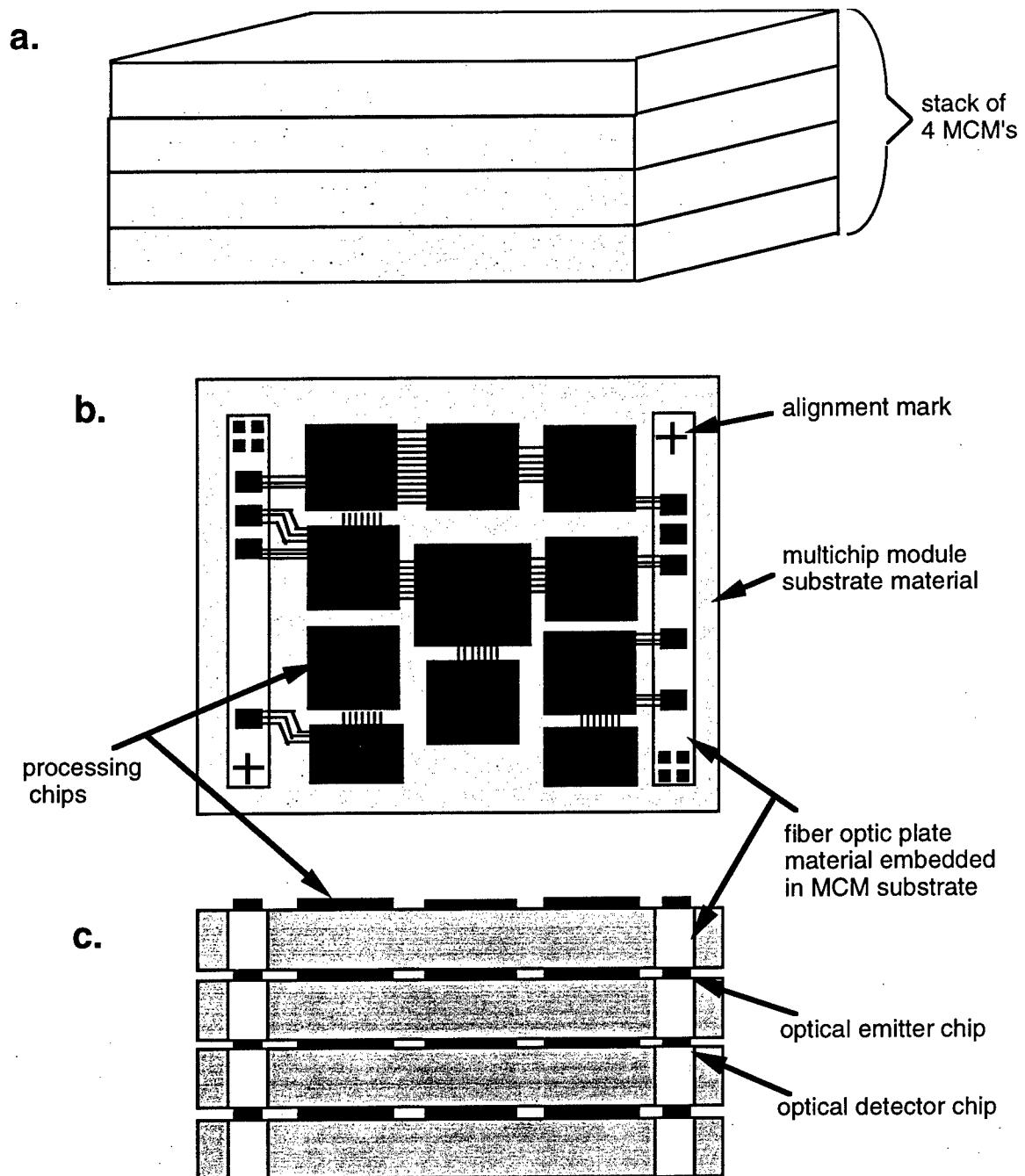
The following report details the achievements made under this program up to the point of program termination. Two applications which drove the development of this technology are briefly described in Chapter 2. Chapter 3 introduces the field of optical interconnects and Chapter 4 explores the use of optically guiding materials in stacked multichip module and chip-scale computers. The detector and emitter arrays designed for the demonstration are discussed in Chapter 5. Chapter 6 discusses the results of a wafer bonding effort for the development of highly efficient emitter and detector arrays.

## **2. Applications:**

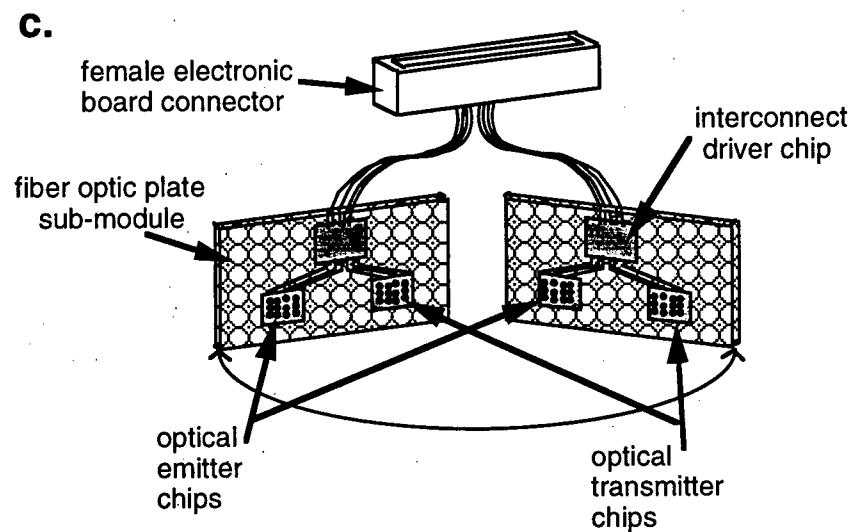
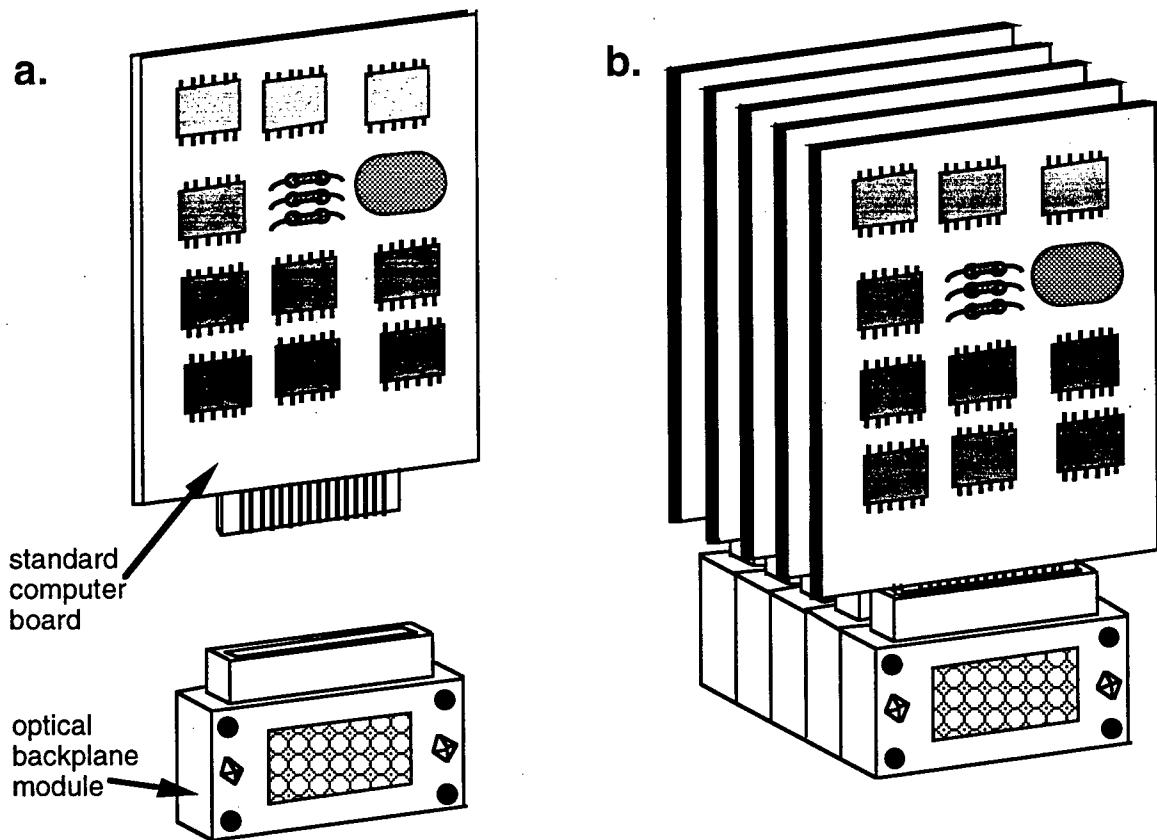
Two applications were identified as insertion points for the optical interconnect technology proposed here. The first falls under the DARPA OMNET effort to develop optical interconnects for enhanced synthetic aperture radar (ESAR) processors<sup>3</sup>. The second application is an optical backplane for the AFRL/IFTE and DARPA/STO Ultra-Comm program. Ultra-Comm is a modular radio system which uses a family of standard PCI/PCMCIA cards to allow for interoperability between a range of military radio systems. An optical data bus is proposed to connect the PCI/PCMCIA cards to provide for high data rates and the isolation required between encrypted and decrypted data streams.

The two applications are depicted in Figures 2.1 and 2.2. Figure 2.1 represents the use of optically guiding material in a stacked multichip module computer

system. This architecture will be explored in detail in Chapter 4 of this report. The use of optically guiding material in an optical backplane is shown in Figure 2.2. In this configuration, standard computer boards are inserted into modules which convert the electronic signals to high speed optical signals which are then transmitted to neighboring modules. The optical backplane modules can be daisy-chained together creating an adaptable, modular computer system. The assembly of the optical backplane module is shown in Figure 2.2.c. Two fiber optic plate modules each with interconnect driver chips and optical emitter and detector chips are mounted chip side-to-chip side and inserted into the backplane module.



**Figure 2.1.** A simplified diagram of optically guiding material used in a stacked multichip module (MCM) computer system. a. represents the stack of MCM's, b. and c. show top and cut-through views of the MCM stack showing the embedded fiber optic plate material.



**Figure 2.2.** A conceptual diagram of optically guiding material used in an optical backplane configuration. 2.a. represents a single standard computer board and a single optical backplane module. In 2.b. five boards have been inserted into the backplane modules and the modules have been assembled into a high speed optical bus. 2.c. represents the internal construction of the optical backplane module.

### **3. Optical Interconnect Background:**

The use of light as a medium for transmitting information between processing circuitry has been the goal of many research efforts<sup>4-9</sup>. By using light instead of traditional electronic signals propagating down wires, the number, density, and speed of data transmitted can be greatly increased leading to the enhanced performance of Air Force processing systems. However, the implementation of optical interconnects has been stalled by the lack of an adequate means of controlling the propagation of the light between circuitry and by the lack of an efficient means of aligning electro-optical systems.

The limits of electronic interconnects are well documented<sup>10-12</sup>. Wires take up too much space, they can not be placed close to one another without cross coupling of the electronic signals, and they have a characteristic capacitance which limit the rate at which data can be sent. As integrated circuits become faster and as processing systems become smaller, the electronic interconnects become the performance limiting factor of the system.

One of the critical information bottlenecks in a complex electronic system is the board-to-board interconnect. The transmission of electronic signals on a single board has been adequately addressed by the advent of multichip modules (MCM's). Bare integrated circuit die are placed next to each other to reduce the distance that electronic signals must travel. However, when a number of MCM's are stacked together to construct a complete computer system<sup>13</sup>, the traditional electronic methods of transmitting signals between modules are limited in the number, density, and data rate of the wires that make up the data paths.

Optical interconnect architectures have been proposed to address this board-to-board data transmission problem. Any optical interconnect scheme must meet certain design requirements. The scheme must provide for the propagation of the optical signals from one board to another in a controlled manner. Light in one

data path must not end up in another data path at the receiving board resulting in a confusion of the transmitted signals. Enough light must be received at the receiving board to discern the data transmitted. The method of aligning the boards during the construction of the computer system must be within the capabilities of the system manufacturers. The alignment of the boards must be maintained through reasonable vibration and heating cycles of the system.

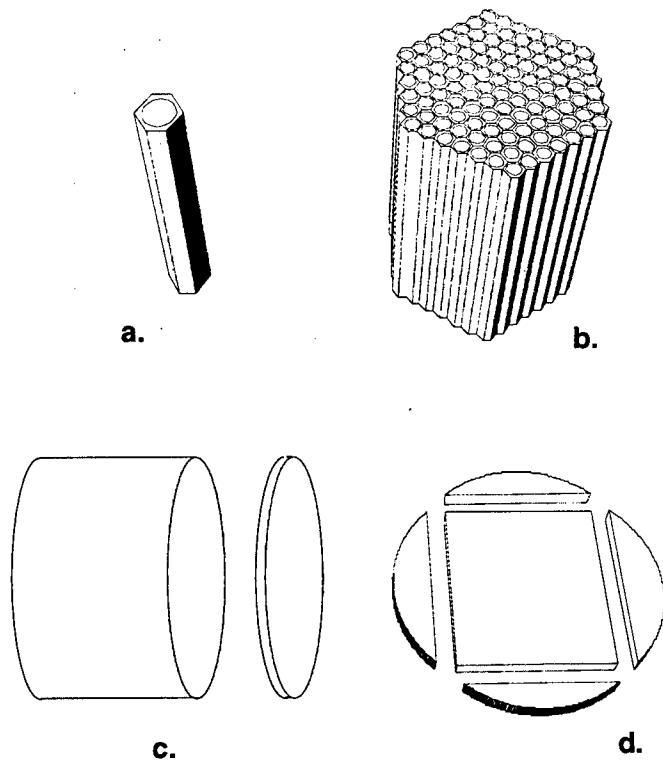
Typically, the interconnect scheme would consist of optical emitters, photodetectors and a lens system which could be a refractive lens, a diffractive optic element or a holographic element. Either a single high speed emitter and detector system or a plurality of many slower emitters and detectors would be placed on each board. The lens would collect the light emitted from one board and focus it onto a detector on another board. In some designs more than one optical lens device is used to control the collection and redirection of the optical signals between boards. The resulting optical interconnect scheme is typically expensive to manufacture and extremely hard to align and is susceptible to misalignment due to jarring or thermal expansion of any of the elements. Optical interconnects have not developed into a commercially viable technology due to the cost and complexity of the schemes proposed. There exists a need for a method of transmitting optical signals from one computer board to another in a controlled manner that is easily aligned.

#### **4. Proposed Optical Interconnect Design:**

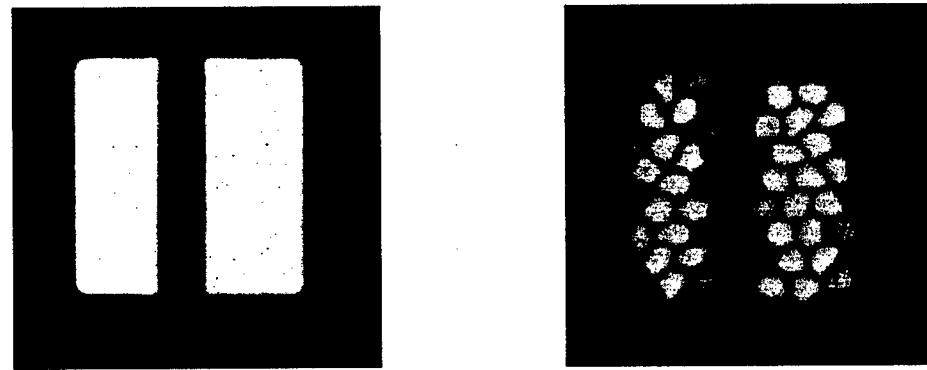
Our goal was to demonstrate a 32-channel optical data bus between MCM substrates with each channel on 125 $\mu$ m centers and each channel operating at 500Mhz. This architecture is scaleable to much greater numbers of interconnects. Our architecture is free from costly micro-lensing devices and has greatly relaxed alignment tolerances compared to other optical interconnect schemes and industry alignment capabilities. The interconnect allows for the use either VCSEL or LED arrays.

The basis for our architecture is the integration of optically guiding material directly into the electronic circuitry support substrate. The material, called fiber optic plate (FOP), is made up of fused optical fibers of 6 to 8 $\mu$ m diameters which run normal to the plane of the material. Figure 4.1 depicts the fabrication of the fiber optic plate, a commercially available product. This material acts as the optical system guiding light from emitters to detectors as well as aiding in the alignment of the circuit boards (modules) to each other. The guiding nature of the material translates any optical image from one side of the module to the other as shown in Figures 4.2 and 4.5. The light from emitter arrays is guided with little distortion to the other surface of a module onto which a corresponding array of photodetectors has been placed. Figures 4.3 and 4.4 show the implementation of this architecture in a single module and the stacking of six modules.

The light guiding nature of the fiber optic plate allows for a high density of data channels. Channel density is limited by how well the interconnect scheme isolates the individual light beams which carry information. Light from a single optical source will enter one or more fiber of the fiber optic plate and will be confined to those fibers until the light reaches the opposite side of the plate. The confinement of the optical signals prevents the divergence of the optical beams which would occur if the light was free to travel through air or a uniform transparent medium.

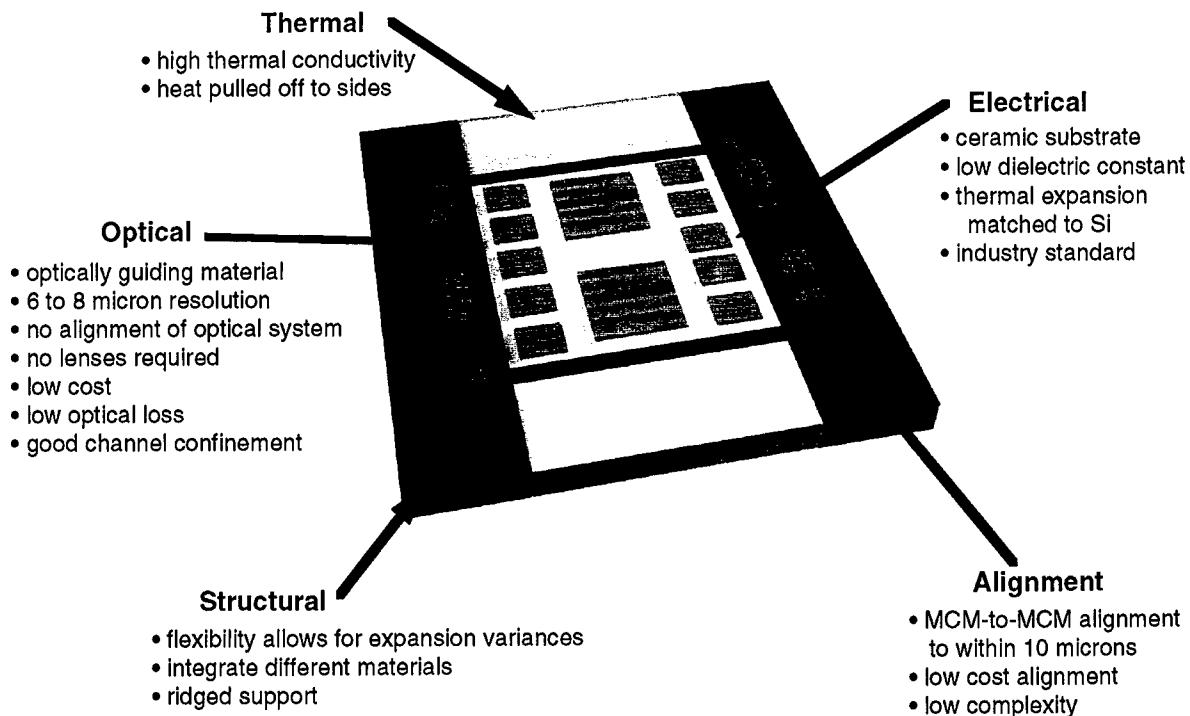


**Figure 4.1.** Fabrication steps of a fiber optic plate: a) fabricate a fiber preform and boule with large core to cladding ratio; b) fibers stacked, fused, heated and drawn; c) drawn fibers are cut, stacked, fused and drawn until desired core diameter is reached; e) final fiber optic bundle is sliced into plates.



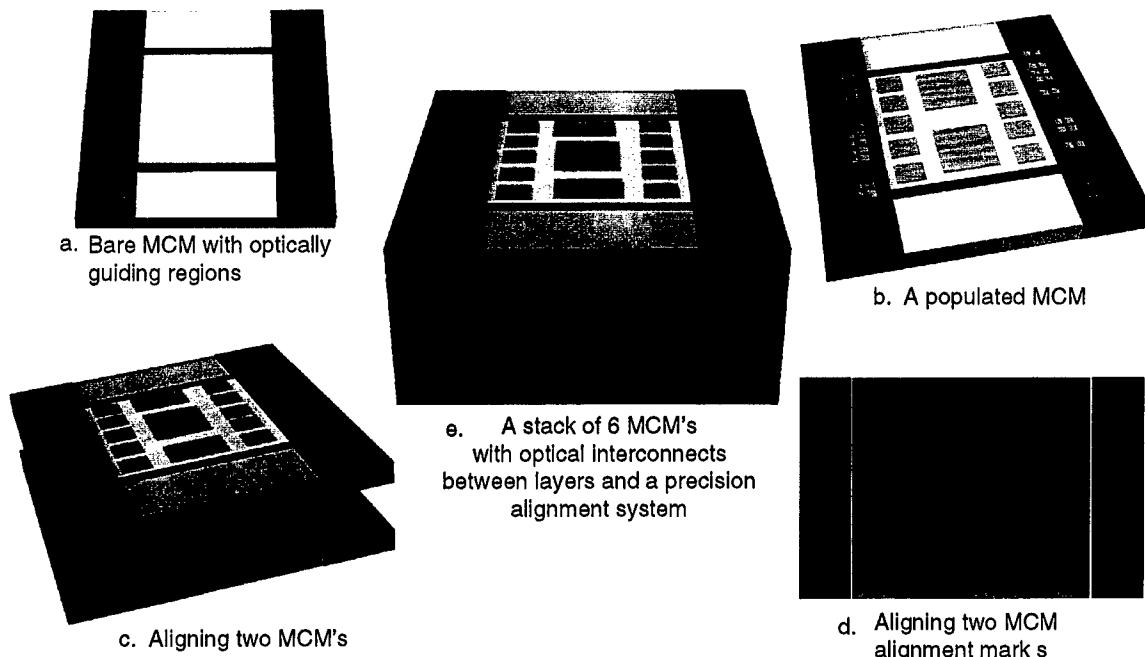
**Figure 4.2.a** Optical micrograph of a,  $50 \mu\text{m} \times 50 \mu\text{m}$  LED. The center stripe is an electrical contact.

**Figure 4.2.b** Optical micrograph of the same LED covered with a 3 mm thick fiber optic plate.



**Figure 4.3.** A conceptual view of a multichip module incorporating a center electronic module and embedded fiber optic plate in areas requiring module-to-module interconnects and alignment marks.

A critical factor in the successful implementation of any optical interconnect scheme is the ease of aligning the components. Unlike optical interconnect schemes which use lenses, diffractive optics or holograms to redirect or refocus divergent light beams, the fiber optic plate does not have to be aligned to the optical source or the optical detector. The light guiding material is part of the support structure of the electronic circuitry. There is no need, as is the case in other optical interconnect schemes, to align a separate optical device to perform an optical guiding or focusing function. The uniform distribution of fibers making up the fiber optic plate simply needs to be placed between the optical emitter and optical detector. It does not matter which fibers carry which optical signals.

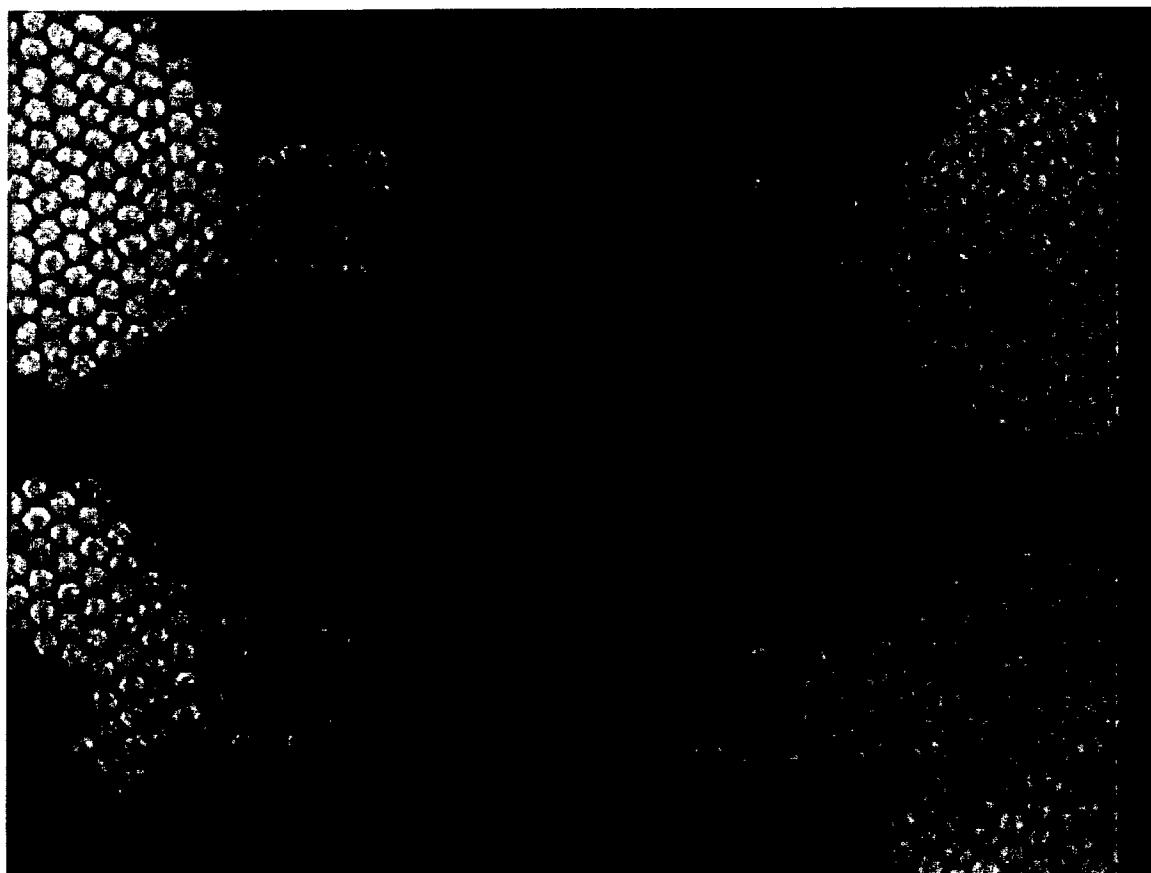


**Figure 4.4.** A conceptual diagram of a) a single multichip module with areas suitable for optical interconnects, b) an MCM populated with IC's, c) the process of aligning two MCM's, d) a method of using complimentary alignment marks on each MCM to align one to another, and e) a stack of 6 such MCM's.

A second factor which greatly eases the task of aligning one optically guiding module to another is the capability to see through the fiber optic plate so that one plate can be aligned to alignment marks on the plate below it. This capability can be enhanced by the use of a light source placed below the two plates or by optical emitters on the first plate. Alignment to within the core size (approximately 6 to 10 $\mu$ m in diameter) of the individual fibers which comprise the fiber optic plate is possible.

The optically guiding module is a lower cost solution to providing optical interconnects for electronic processors than most other schemes. No complex and costly optical devices such as refractive lenses, diffractive optics, or holograms are required. Also the guiding nature of the proposed substrate allows for the use of low cost light emitters such as light emitting diodes while not precluding the use of other types of light emitting devices. Many other

interconnect schemes depend on the narrow beam emissions from expensive and environmentally unstable vertical cavity surface emitting lasers (VCSEL's).



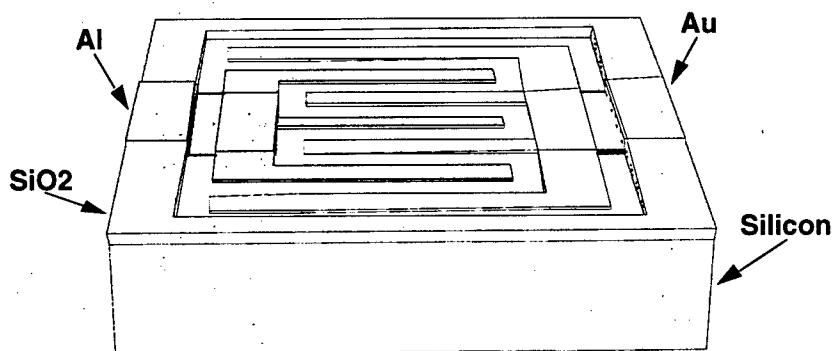
**Figure 4.5.** Optical micrograph of a fiber optic plate material placed over an array of vertical cavity surface emitting lasers with the upper left laser turned on. The fibers effectively guide the light from the  $10\mu\text{m}$  diameter source output. The lasers are separated by  $125\mu\text{m}$ .

The ability of the fiber optic plate to efficiently collect the light from a source and guide the optical image to a detector with little distortion reduces the power required to transmit information and reduces crosstalk. The proposed interconnect has a higher efficiency than diffractive optic and hologram based systems. Also, the free-space nature of optical interconnects may create more reliable systems due to the replacement of solder connections that are prone to thermal cycle induced cracking and pressure-contact interconnects which are prone to wear.

## 5. Optical Interconnect Device Development:

### 5.1 Metal-Semiconductor-Metal Photodetectors:

Metal-semiconductor-metal (MSM) photodetectors were chosen for our interconnect scheme due to their monolithic design, integratability with standard VLSI circuitry, high speed performance, and applicability to 2-D array layouts<sup>14-20</sup>. Silicon was chosen as the detector substrate due to compatibility with CMOS circuitry and the availability of mature light emitting diode and vertical cavity surface emitting laser device technologies that emit light in the silicon sensitivity bandwidth. A two-metal design was chosen to reduce dark current and two detector layouts were designed. The function, design, and fabrication of silicon MSM photodetector arrays will be presented in this chapter.

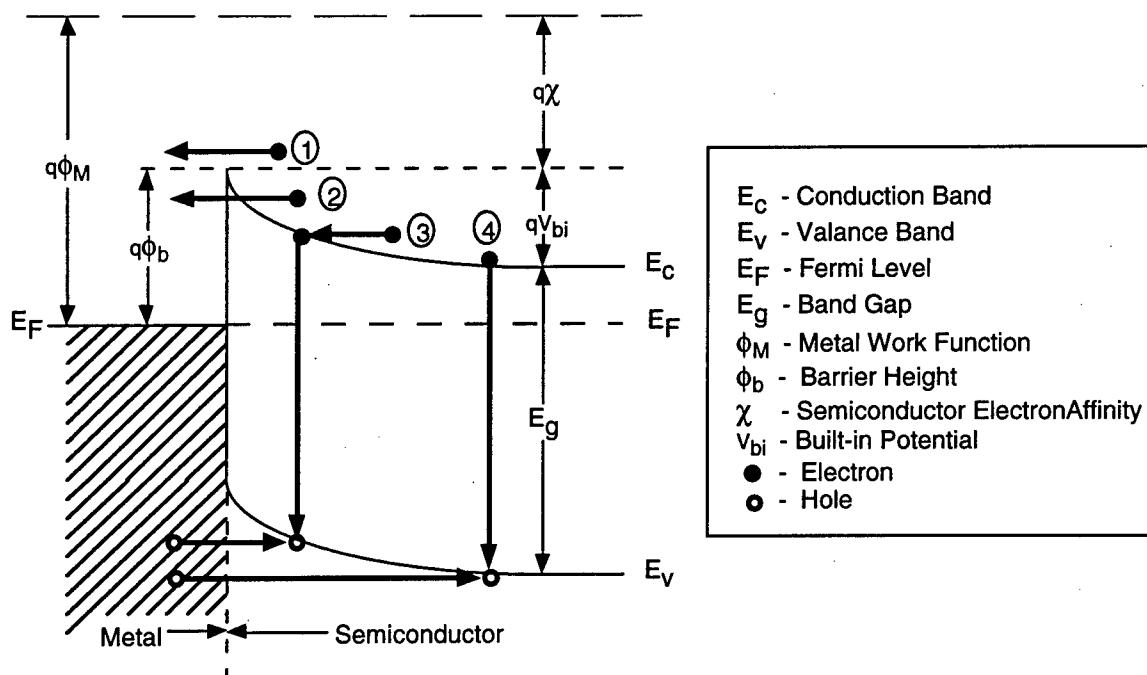


**Figure 5.1.** Metal-semiconductor-metal photodetector layout showing the Si active area, interdigitated metal electrodes, and the  $\text{SiO}_2$  insulation.

### 5.1.1 Device Physics

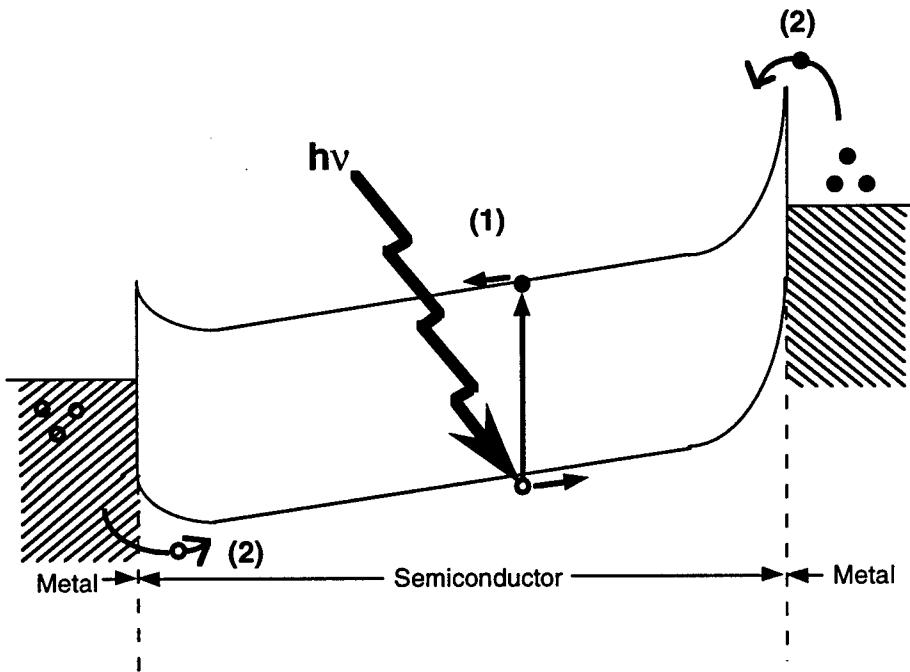
MSM photodetector characteristics are determined primarily by substrate material, electrode metal, processing conditions, and electrode layout. The spectral responsivity of the detector is primarily a function of the substrate material band gap. Device operating speed is dependent on electrode geometry as well as substrate characteristics such as electron and hole mobilities. Dark current is dependent on the characteristics of the rectifying contacts formed between the electrode metals and the substrate material.

Fundamentally, the MSM photodetector is comprised of a pair of biased interdigitated metalizations on a semiconductor surface (see Figure 5.1). The metal-to-semiconductor interfaces form Schottky or rectifying contacts. The combination of the two Schottky contacts create a low noise and highly sensitive photodetector, the physical properties of which will be explained in the following paragraphs.



**Figure 5.2.** Energy diagram of a metal, n-type semiconductor contact showing carrier transport mechanisms<sup>9</sup>.

The current transport processes responsible for both signal and dark current in MSM photodetectors are shown in the simplified metal-to-semiconductor interface energy diagram of Figure 5.2. This figure depicts the forward biased interface with the following carrier transport methods: (1) the transport of photo-generated electrons from the semiconductor to the metal over the potential barrier, (2) the quantum-mechanical tunneling of electrons through the potential barrier, (3) the recombination of electron-hole pairs in the space-charged region, and (4) the hole injection from the metal to the semiconductor<sup>21</sup>. This report is concerned with the transport mechanisms labeled (1), the collection of photogenerated carriers which act as the desired signal and (4), the carriers injection from the metal into the semiconductor which contribute to the dark current.



**Figure 5.3.** Energy-band diagram of a biased MSM detector indicating (1) the photogeneration of signal charges and (2) the thermally-generated carriers overcoming barrier heights adding to device dark current.

Figure 5.3 is an energy-band diagram of the MSM photodetector in the biased state. The vertical displacement of the electrode metals indicates the bias

voltage applied to the device resulting in the forward biased condition of the left-hand metal-semiconductor interface and the reverse bias of the right-hand interface. Upon biasing, the Si between the electrodes becomes fully depleted of free carriers. The reversed biased interface prevents current from flowing through the device in the absence of an optical signal. The depleted regions between the electrodes are the photodetector active regions. A photon with a photon energy greater than the band gap of Si (1.12eV) will be absorbed by an electron exciting it to the conduction band as shown by the process labeled as (1) in Figure 5.3. The photo-generated electron and hole are swept by the high applied fields to the positive and negative electrodes resulting in an electronic output signal.

As depicted in Figure 5.3 (labeled with a (2)) there is leakage current due to thermally excited carriers which make it over the barrier in the case of electrons ( $J_n$ ) from the negative electrode and under the barrier in the case of holes ( $J_p$ ) from the positive electrode<sup>15</sup>. The rate of flow of these carriers is determined by the size of the barrier that they encounter at the metal-to-semiconductor interface. In the case of electrons (a similar case can be made for holes) at the negative electrode, a certain percentage of electrons will possess the energy to overcome the barrier and enter the semiconductor and thereby add to the dark current of the system. The probability that an electron will have an energy, E can be approximated by the Fermi Function:

$$f(E) = \frac{1}{1 + \exp (E - E[f]) / kT} \equiv \exp -(E - E[f]) / kT$$

for  $E > (3kT + E[f])$  where  $E[f]$  is the Fermi energy,  $k$  is Boltzmann's constant, and  $T$  is temperature in degrees Kelvin. The number of electrons with energies greater than the barrier height decreases exponentially with the increase barrier height. Therefore, increases in barrier height can be used to decrease the

detector dark current<sup>22</sup>. The current contribution of electrons emitted over the barrier from the metal to the semiconductor is defined by Bethe's thermionic emission theory:

$$J_{ms} = \frac{pqN_c(8kT/\pi m^*)^{1/2}}{4 \exp(-q\phi_b/kT)}$$

where p is the fraction of electrons tunneling from the semiconductor to the metal, q is the electron charge, N<sub>c</sub> is the effective density of states in the semiconductor conduction band, m\* is the effective mass of electrons in the semiconductor, and  $\phi_b$  is the metal-semiconductor interface barrier height. Again, we see that the current decreases exponentially with respect to increases in the barrier height<sup>23</sup>.

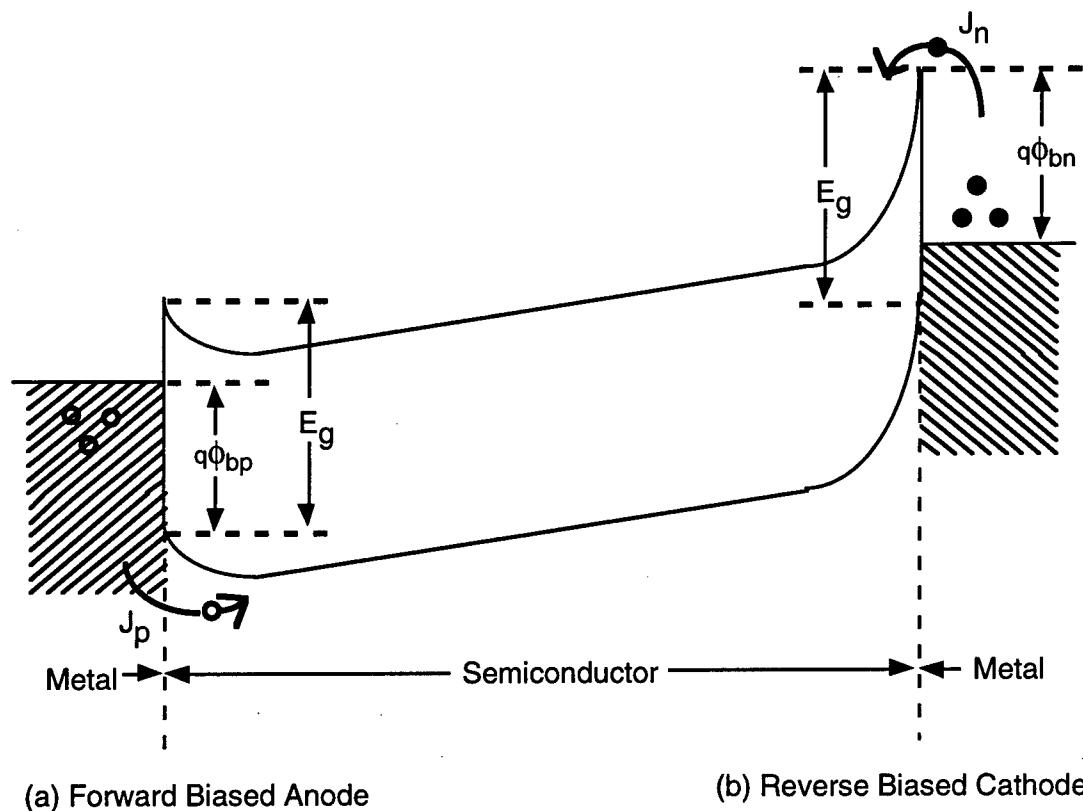
The barrier height,  $\phi_b$ , of the metal-semiconductor interface can be approximated from the electron affinity of the semiconductor,  $\chi$ , (the energy needed to take an electron from the conduction band to vacuum), and the metal work function,  $\phi_M$ , (the energy required to take an electron from the metal Fermi level to vacuum). This can be seen in the energy diagram of Figure 5.2 and is represented by the following equation (barrier lowering due to the Schottky effect is ignored here for simplicity):

$$\phi_b = \phi_M - \chi$$

The semiconductor affinity is a characteristic of the semiconductor material and doping, both factors are fixed by industry standards for low cost Si wafers. The choice of metals, and therefore, the choice of metal work functions is more variable. The main constraint on the choice of a metal is that it must form a rectifying contact with the semiconductor substrate. To meet this requirement the metal work function ( $\phi_M$ ) must be greater than the semiconductor work

function (n-type Si with a doping level of  $8 \times 10^{14} \text{ cm}^{-3}$  has a work function of 4.32eV).

A large value of  $\phi_b$  will limit the number of thermally excited electrons which pass from the negative electrode to the semiconductor. Likewise a small  $\phi_b$  value will result in a greater barrier for holes passing from the positive electrode to the semiconductor. This can be seen in Figure 5.4, note that the semiconductor band gap  $E_g$  is a constant. If different metals are used for the positive and negative electrodes, then the barrier heights can be optimized to reduce the number of either electrons or holes which acquire enough energy to overcome the barrier thereby reducing the device dark current.



**Figure 5.4.** Energy band diagram of an MSM photodetector showing (a) the positive electrode, forward biased interface and (b) the negative electrode, reverse biased interface. Different metals form different barrier heights to prevent unwanted hole ( $J_p$ ) or electron ( $J_n$ ) transport into the semiconductor.

### **5.1.2 Two-Metal Electrode for Lower Dark Current:**

Aluminum (Al) and gold (Au) were chosen as the positive and negative detector electrodes, respectively. Both metals are common VLSI materials and have work functions greater than the Si work function of 4.32eV (4.55 for Al and 4.86 for Au). The barrier height for Al-Si interface is 0.50eV resulting in a 0.62eV barrier for the holes to pass "under". The Au-Si interface results in a 0.81eV barrier height for the electrons to pass "over".

The above description of the metal-semiconductor interface dynamics is, however, an idealized model. Three factors which may upset this model are the effects of surface states in the semiconductor, imprecise work function figures, and the presence of a significant interfacial layer. The presence of surface states in the semiconductor play a major role in dictating the location of the Fermi level at the metal-semiconductor interface. If the density of surface states is high, then the Fermi level will be "pinned" to an energy level determined by the doping of the semiconductor and the properties of the surface states and the Schottky barrier height will be defined by the following equation:

$$q\phi_b = (E_g - q\phi_0) - q \Delta\phi$$

Where  $\phi_0$  is the energy level at the semiconductor surface which is heavily influenced by surface states and  $\Delta\phi$  is the image force barrier lowering due to the Schottky effect<sup>21</sup>. Note that the barrier height is no longer influenced by the metal work function. The processing conditions used to clean the semiconductor surface before metal deposition play a major role in the creation of surface states.

The usefulness of the dual metal technique depends on the ability to "design" a barrier height by choosing a metal with a known work function for use in a Schottky barrier. Unfortunately, barrier height values vary greatly by the method

of surface preparation, metal deposition, and the test environment<sup>23</sup>. Idealized values are obtained by cleaving semiconductors in vacuum and depositing metal onto the clean surface. The variation in surface cleaning and metal deposition technique between the researcher tabulating barrier height tables and the manufacturer of devices often results in differing results. It is not feasible to construct photodetectors under the idealized conditions used to determine the metal-semiconductor barrier height. Contamination of the surface due to wet chemical and air exposure results in increased surface states and the formation of an interfacial oxidation layer which results in further departure from the idealized model.

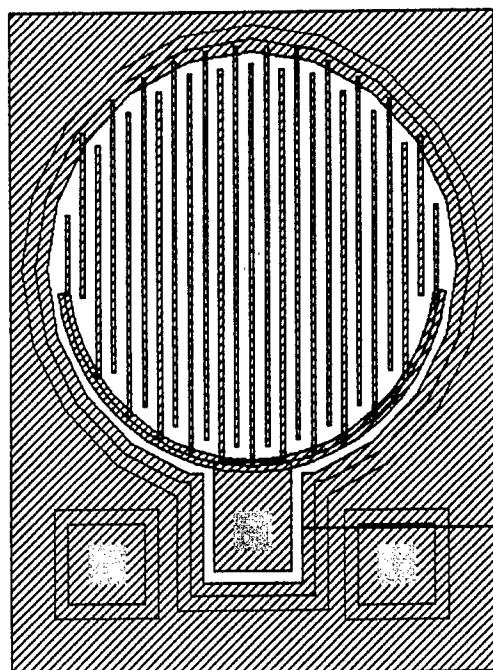
### **5.1.3 Photodetector Die Layout:**

Two photodetector configurations were designed for the interconnect demonstration. Physical layouts for both designs were finalized and drawn out in a CAD program as shown in Figure 5.5. With the continued funding of this program, both detector arrays will be fabricated in silicon, packaged in a test module and tested as part of a 32 channel module-to-module optical interconnect. The detectors shown in Figures 5.5.a and 5.5.c are a 2X16 array of 100 $\mu\text{m}$  diameter detectors on 125 $\mu\text{m}$  centers. Digit width is 1 $\mu\text{m}$  with 3 $\mu\text{m}$  spacing between digits. The annular detectors shown in Figures 5.5.b and 5.5.d are 100 $\mu\text{m}$  diameter devices with a 30 $\mu\text{m}$  center hole. Digit width and spacing is also 1 $\mu\text{m}$  and 3 $\mu\text{m}$  respectively.

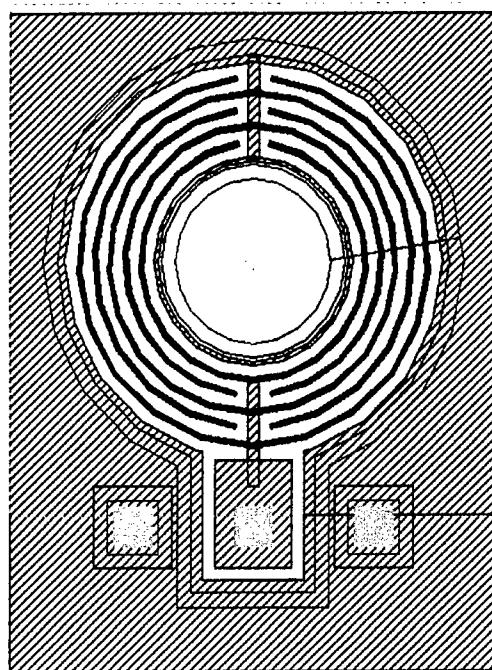
The annular detectors were designed for silicon-on-fiber optic plate or silicon-on-sapphire wafers. A 3 to 5 $\mu\text{m}$  thick layer of silicon bonded to a transparent substrate (or optically guiding substrate) would create a detector chip that could receive light from the top or bottom. The guiding nature of the fiber optic plate would channel optical signals from the chip backside directly to the receiving detector. The annular detectors could be assembled in a stack such that each detector picks off a percentage of the transmitted optical signal. The size of the

hole is dependant on the expected divergence experienced between each detector and the amount of light required for each detector. Such a configuration would enable a single emitter to broadcast a signal to a number of layers as in a clock distribution system.

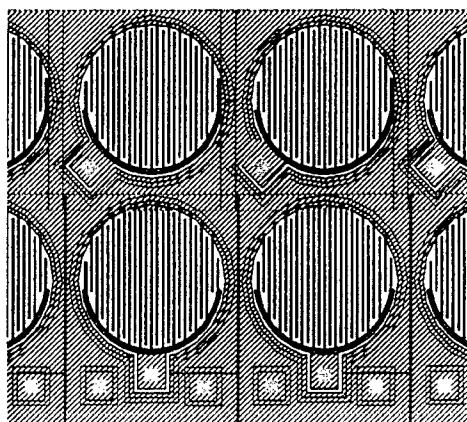
a.



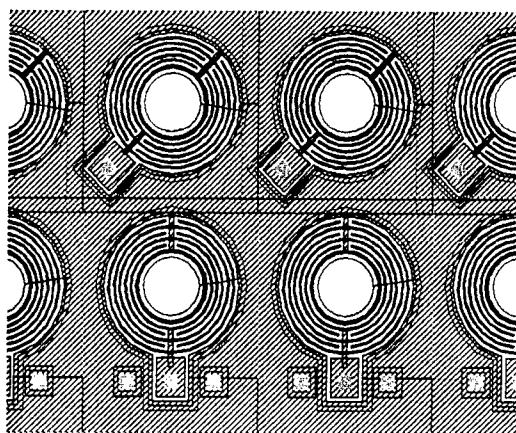
b.



c.



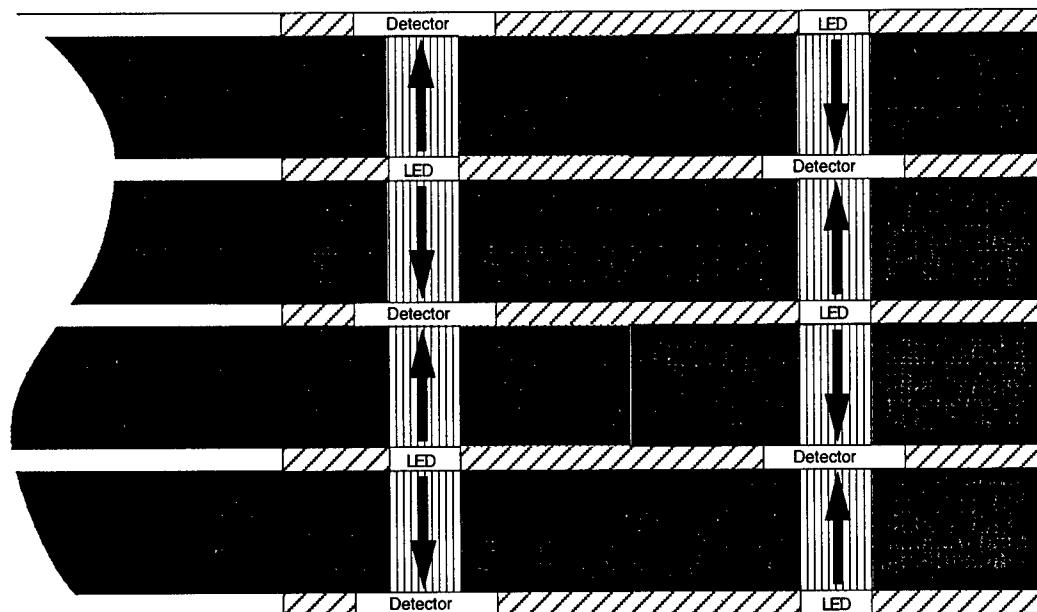
d.



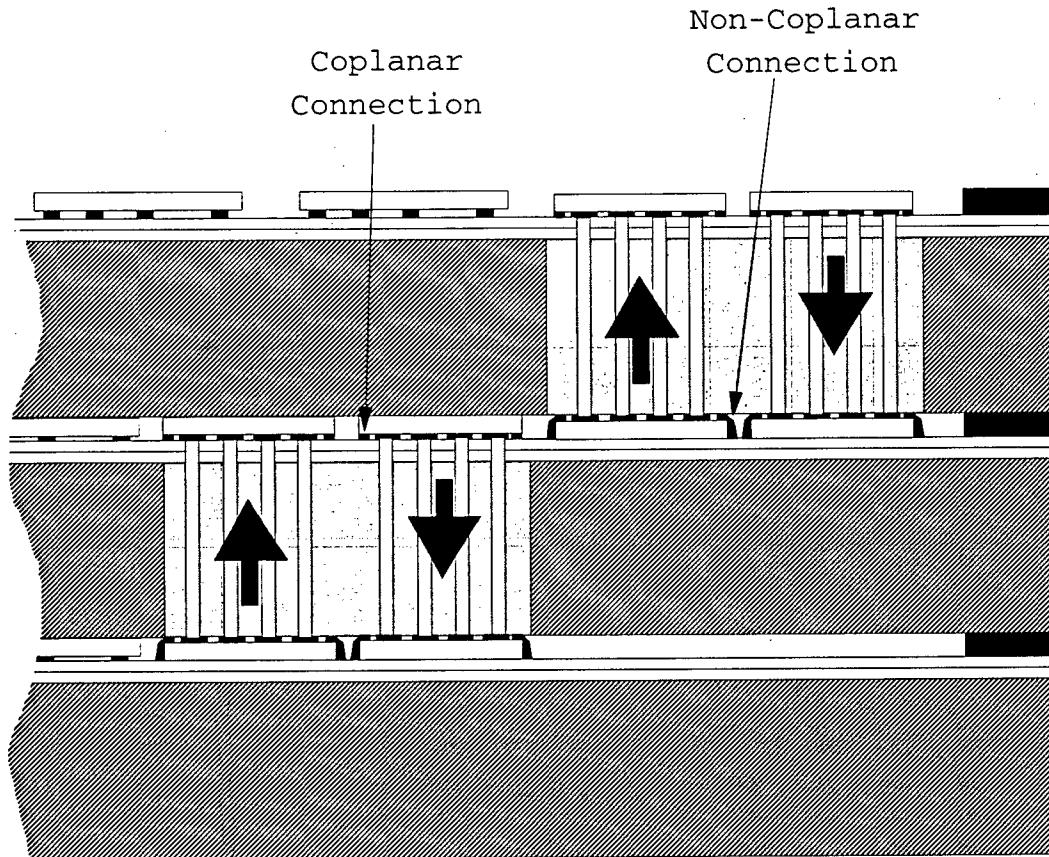
**Figure 5.5** Computer aided design (CAD) layouts of metal-semiconductor-metal (MSM) photodetectors. Single and arrayed devices are shown for the standard (a. and c.) and the annular (b. and d.) detector designs.

## 5.2 LED Design and Fabrication:

The use of fiber optic plates (FOPs) to move signals from level to level allows the system designer to consider using LEDs as emitters rather than VCSELs. Normally an LED would not be useful in the application considered here because the LED is basically a Lambertian source; it emits light in all directions and so the light cannot normally be directed from one location to another in an efficient manner. However, the fibers that make up the FOP have a high numerical aperture that allow them to collect most of the light from the LED, under the assumption that the FOP and LED are essentially in contact. This light is then channeled down a group of fibers to a detector in next level of circuitry (Figure 5.6).



**Figure 5.6.** The proposed optical bus channels the light from layer to layer by use of Fiber Optic Plates (FOPs). The thinned LEDs and detectors are inherently detecting/emitting on both upper and lower sides and this is utilized to reduce the number of needed devices and to simplify electrical connection as discussed.



**Figure 5.7.** An optical bus scheme similar to the one shown in Figure 5.6 but using unthinned chips (chips with their substrate attached that make them opaque in that direction). The emitter/detector pair on the left in the middle layer are attached so that the metal electrical contacts are downward facing which allows normal coplanar flipchip contacts to be made. The upward facing chips in the same layer on the right have non-coplanar contacts; there is no easy way to make the 0.5 mm vertical trace to connect them while also connecting the downward facing chips.

The emitter and detector arrays will be flip chipped onto FOP substrates patterned with metal traces for electrical connection. These chips will then have their substrates removed by thinning so that they can emit/detect from both sides. If the chips were flip chipped and not thinned then two sets of emitters/detectors would be needed: one to emit/detect up and one to emit/detect down as shown in Figure 5.7. This would present a problem with electrical connection of the chips emitting/detecting upward because the metal electrical traces would have to move from the FOP metal traces to the contact pads on the upward facing chips which is a distance of about 0.5 mm. There is no immediate

solution that would make this connection and also the connection for the downward facing chips and also allow optical transmission of light in both directions.

Although an LED is currently limited to about 500 MHz frequency response it is felt that the use of LEDs in this application should be pursued because LEDs are inexpensive, robust, and easy to fabricate. The physical reason for the limited speed of LED is the lifetime of the charge carriers. There are methods by which this limitation may be removed for a substantial increase in speed. The other alternative, VCSELs, although they can be modulated at 10 Gbps, are expensive, difficult to make (especially in large arrays, as required by this application), and can only be operated over limited temperature regimes. In addition the efficiency of current production VCSELs is only about 10% (Power in/Power out) because of high resistance contacts whereas an LED with its substrate removed may be several times as efficient. Another problem with VCSELs is that they will only turn on when at least ~1 mA is applied to them. This results in a light output of about 1/2 milliwatt. This is about an order of magnitude more light than is needed for the optical interconnect scheme discussed in this report and therefore will result in an order of magnitude increase in power dissipation. The LED does not exhibit this lower limit of operation and hence can be operated in the 100 \_W regime without difficulty. Finally, the physical reason for the VCSEL's speed limitations are the narrow optical bandwidth inherent to its lasing action. This bandwidth limit sets an upper limit on how fast the VCSEL can be turned off and on for digital applications (20 Gbps) and, it's felt, is a more fundamental limitation than the speed limitations of current LED's. This said, we also have VCSEL arrays in hand both as a fallback position and to immediately demonstrate the high speed capabilities of our Fiber Optic Plate approach. An advantage of the approach described is that it will work equally well with both VCSELs and LEDs.

Previously, the Optical Interconnects Group fabricated GaAsP surface emitting LED arrays as part of its initial effort at an optical interconnect architecture<sup>25</sup>. These LEDs were designed to emit at 655 nm and were single heterostructure devices. Among the other problems these LEDs had were the fact that they were very inefficient. A new design attempts to correct this shortcoming.

The new LED design is a double heterostructure device that should yield internal efficiencies of at least 80%. Assuming this is achieved, getting this light out of the device becomes the main problem. The difficulty lies in the fact that the index of refraction of the AlGaAs is about 3.4. The angle of total internal reflection into air is then

$$\theta_1 = \text{Arcsine} \left( \frac{n_1}{n_2} \right)$$

where  $\theta_1$  = Angle of Total Internal Reflection

$n_1$  = Index of Refraction of first material

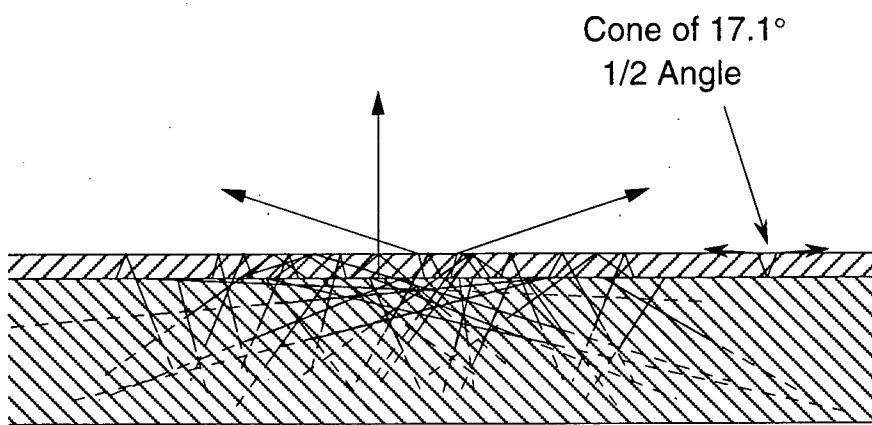
$n_2$  = Index of Refraction of second material

$$\text{Arcsine} \left( \frac{1}{3.4} \right) = 17.1^\circ$$

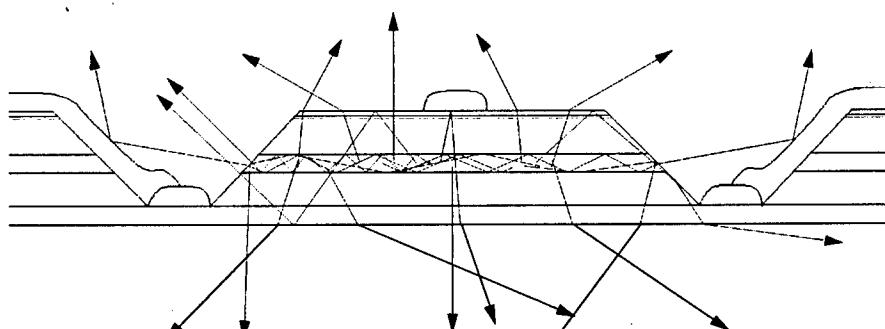
This is the half angle for the cone of light that would be emitted from one surface of the LED. Since in our previous surface emitting LED structure the light was emitted from only one side (surface) we can calculate the percentage of light that would be emitted by using this number. Integrating over a cone whose half angle is  $17.1^\circ$  yields  $0.08846\pi$  as opposed to  $4\pi$  for all angles. The  $17.1^\circ$  cone then represents  $0.08846/4 * 100 = 2.2\%$  of the light escaping the device; the rest is absorbed in the substrate (See Figure 5.8.a). This, and a low internal quantum efficiency, helps explain why the output of original devices was so low (about

$3\mu\text{w}$  at 10ma yielding a QE of about 0.75%). The new devices shown in Figure 5.8.b will allow most of the light to escape (~90%) and will have a very high internal QE (~80%). The use of low resistance topside contacts will yield an overall power efficiency of about 70%. An efficiency of 70% would be several times that of currently available LEDs.

One might be tempted to criticize the above design by pointing out that high efficiency is achieved by counting the light that is propagated both up and down as legitimate output. This is not a false economy because to do the same task of transmitting both to an upper layer and transmitting to a lower layer with conventional emitters would require two chips -- one pointed up and another pointed down (compare Figures 5.6 and 5.7). The current for the chip pointing up would be  $I$  and the current for the chip pointing down would be  $I$  for a total drive current of  $2I$  (Figure 5.7). The proposed two sided device (Figure 5.6) would replace these two by one emitter transmitting both up and down simultaneously and driven with a current of  $2I$ . So one can see that the drive current is the same, assuming equal efficiencies for the sake of this argument, that the light output is the same, and that the proposed two sided LED does the job of two conventional LEDs. In addition it should be pointed out that if one used two conventional one way emitters that while one of the chips could be mounted conventionally, say, by flip chip mounting, the electrical connection of the other chip would be problematical as the chip contacts and the circuit traces of the circuit board or module would not be coplanar (see Figure 5.7). The proposed two sided LED can be mounted by whatever way is most convenient, probably flip chipping.



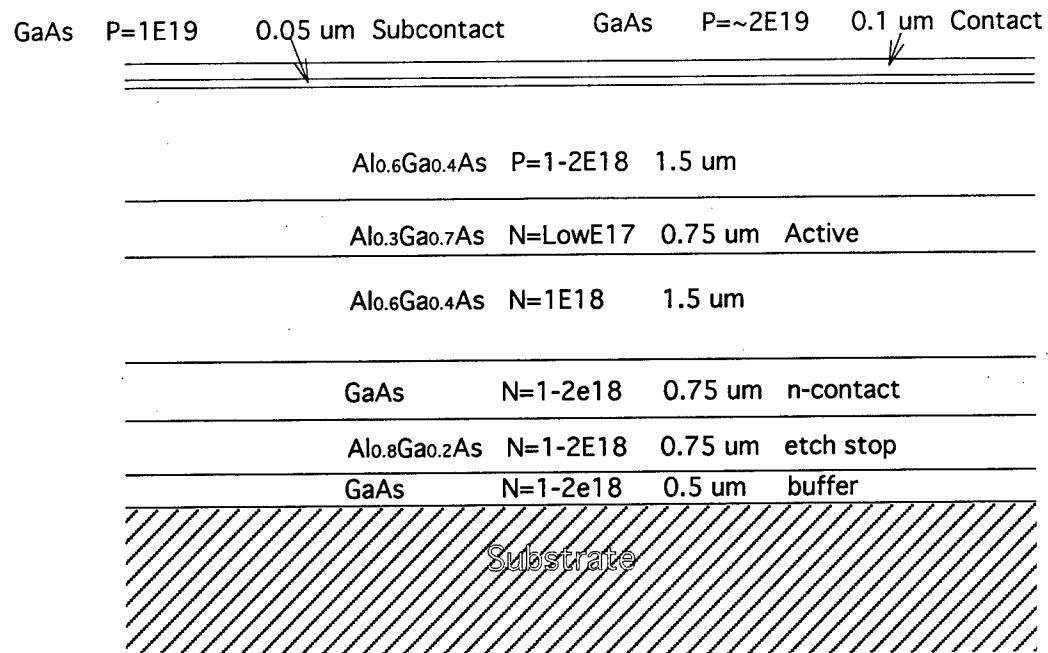
a



b

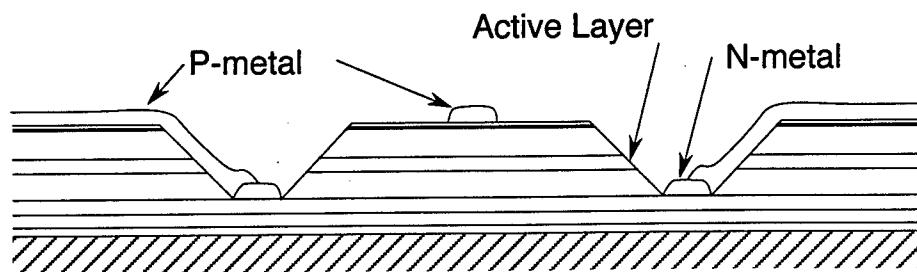
**Figure 5.8.** a) shows the 1st attempt at an LED. Most of the light generated is absorbed by the substrate. b) shows the new structure emitting from both sides. Substrate removal and a mesa structure allows the majority of light to be emitted.

The proposed design uses a double heterojunction as shown in Figure 5.9. This is a straight forward structure that is easily grown and can be obtained from any AlGaAs epitaxial wafer supplier.



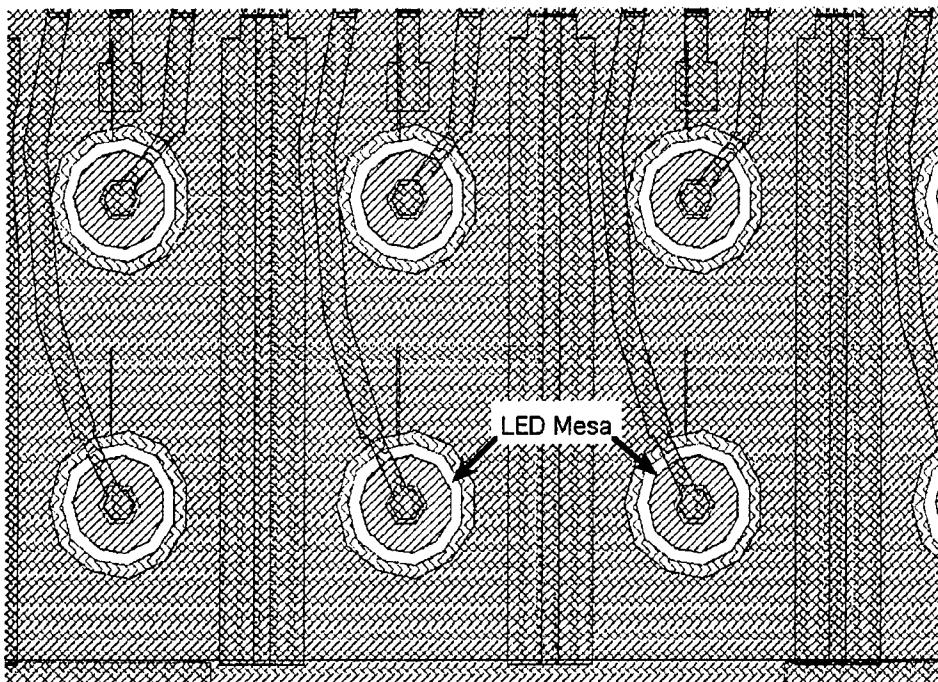
**Figure 5.9.** The LED uses a conventional double heterojunction structure.

Figure 5.10 shows the finished profile (or crosscut) of the device. The figure illustrates the trenches cut to define the active mesa and the N-metal and P-metal contacts. Figure 5.8.b shows how the light generated in the active region will escape the device. The P-metal deposited on the outer sides of the trench will help reflect light emitted directly from the sides of the mesa structure into an upward direction. Approximately 50% of the light will be emitted upward and 50% will be emitted downward.

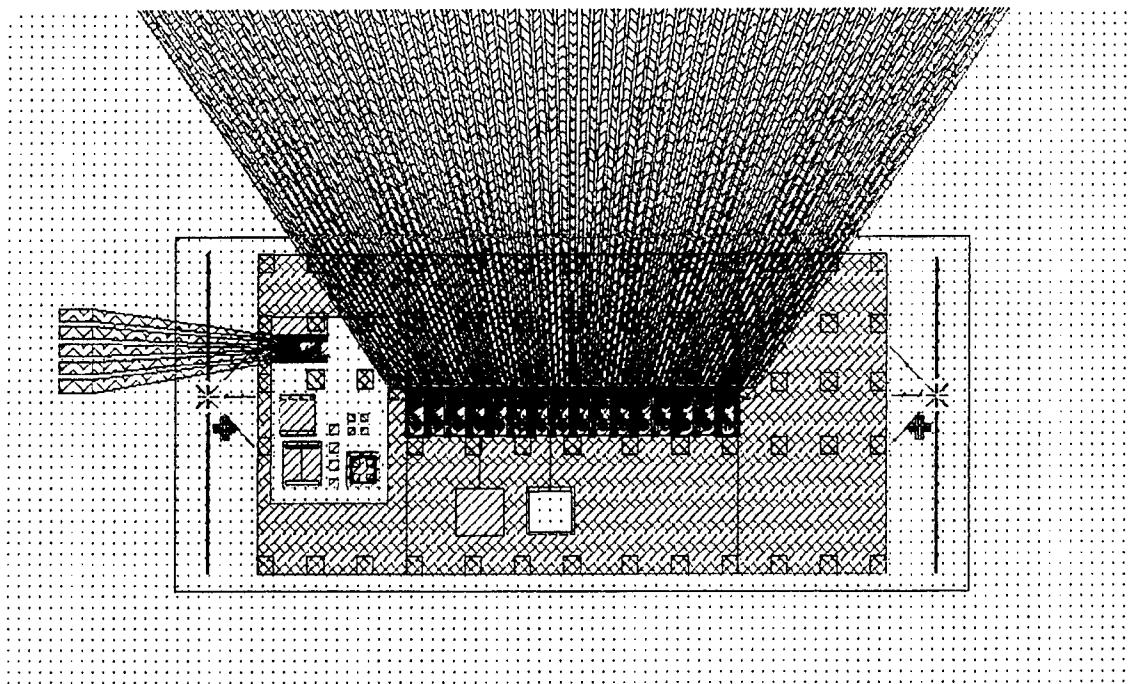


**Figure 5.10.** LED mesa profile

Figure 5.11 shows a view of the mesa from above. This view is from a CAD drawing used to make the mask set for a 2 x16 array of LEDs. The wires leading from the center of the mesas up and out of the frame are part of a header metal pattern that will be deposited and patterned on a glass Fiber Optic Plate (FOP). The LED array will be flip chipped onto the patterned FOP; the header connections will fan out for external high speed testing of the LED arrays. A zoomed out view of the chip and header is shown in Figure 5.12. The chip is about 5mm x 2mm and the header fans out to the edge connector pads that are



**Figure 5.11.** Top view of LED mesas.



**Figure 5.12.** LED chip with header fanning out to the top of the picture. The chip dimensions are about 5 x 2 mm and the header eventually fans out to 75 mm.

75mm wide and so cannot be shown here on the same scale. The small header on the left is connected to two test LEDs and fans out to connectors on 100 um centers. This will allow testing of the LEDs up to 1 GHz and beyond using Cascade probe tips. Near the two test LEDs are other test structures that will be used to characterize the fabrication process.

Processing of the LED wafers will closely follow the process previously worked out for VCSEL fabrication in a previous project<sup>26</sup> as part of the Optical Interconnects Group.

## **6. Wafer Bonding**

### **6. Introduction to Wafer Bonding:**

Much of the wafer bonding work followed the work of Duke University researchers Tong and Gosele. They developed a method for hydrophilic bonding Silicon and glass in a microcleanroom environment. The initial cleaning of the wafers and formation of a hydrophilic surface are done by a method first reported by Kern and Puotinen of RCA corp., and still widely used today. The two step, two solution cleaning method takes care of both organic contamination and heavy metals, as well as leaving dangling OH hydroxyl radical groups, making the surface hydrophilic.

Hydrophobic wafer bonding can also be used, however, this technique involves the use of Hydrofluoric acid (HF), which is particularly caustic and requires that samples be annealed at higher temperature to achieve the same bond strength as hydrophilic bonding. Since silicon and glass have very different thermal expansion coefficients ( $2.56 \times 10^{-6}/^{\circ}\text{C}$  for Si<sup>29</sup>, which is in agreement with other published literature<sup>36-40</sup>,  $0.5 \times 10^{-6}/^{\circ}\text{C}$  for fused quartz<sup>29</sup>, and  $8.9 \times 10^{-6}/^{\circ}\text{C}$  for fiber optic plate), lower temperature bonding is necessary to insure low stress at the bond interface.

An alternative approach to wafer bonding, anodic bonding, was briefly considered but rejected in favor of hydrophilic bonding. Anodic bonding relies on Sodium mobility in the glass to form the bond. This was assumed to be undesirable for semiconductor devices especially since fiber optic plate (FOP) has a high sodium concentration. The fiber plate that was used contained 13% Na in the core, and 7% Na in the cladding. Later it was learned that Na+ goes through the glass to the cathode connection on the top of the glass, away from the bond interface<sup>34</sup>. Anodic bonding could still have potentially detrimental effects due to the displacement of various ions. Side affects include Na+ caking

on top surface, pitting from Sodium Hydroxide which is formed from the displaced Na<sup>+</sup>, and 'polarization' i.e. space charge at the bond interface.

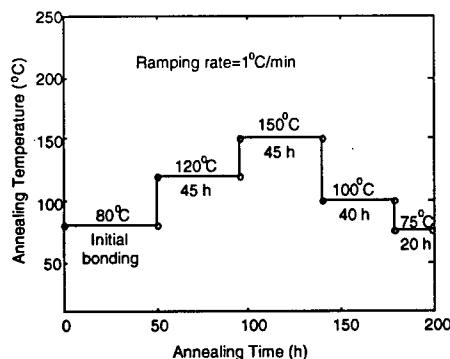
## 6.2 Hydrophilic Si/Glass Bonding

All of the following wet chemistry was preformed at the Cornell Nanofabrication Facility (CNF). Standard RCA1 (NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O = 1:1:5 or 0.25:1:5) solution was used to treat the wafers at nominally 60°C, for approximately 10 minutes. In practice, the temperatures ranged from 75-85°C. RCA1 solution is designed to remove organic contaminants by both solvating action of the ammonium hydroxide and oxidizing action of the hydrogen peroxide<sup>28</sup>. RCA1 also grows a thin (native) oxide layer -- SiO<sub>2</sub>

After the first solution, the wafers are DI rinsed. Standard RCA2 (HCl: H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O = 1:1:5) solution was used to treat only the silicon wafer at 60°C, for approximately 10 minutes. RCA2 removes heavy metals and prevents replating from solution by forming soluble complexes with the resulting ions<sup>28</sup>. Glass was treated in RCA1 only since HCl in RCA2 can attack B<sub>2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub> in borosilicate glass<sup>30</sup>.

After the last solution, the wafers are DI rinsed, and either spin dried or blow dried. At first blow drying with N<sub>2</sub> was done until a spinner was used later. The initial bonding of the wafers is done with slight external pressure at center to initiate contact wave. Optimal initial bonding temperature to reduce thermal stress is T<sub>i</sub> = 86.5°C.

Annealing, up to 150°C, was done at Rome Research site, see ramp schedule below in Figure 6.1. This necessitated the storage of bonded wafers at RT while being transported to Rome. The bonding of the two surfaces is done by a process of desorption of water molecules, which forces the wafers to draw together<sup>29</sup>.



**Figure 6.1** Temperature ramp schedule

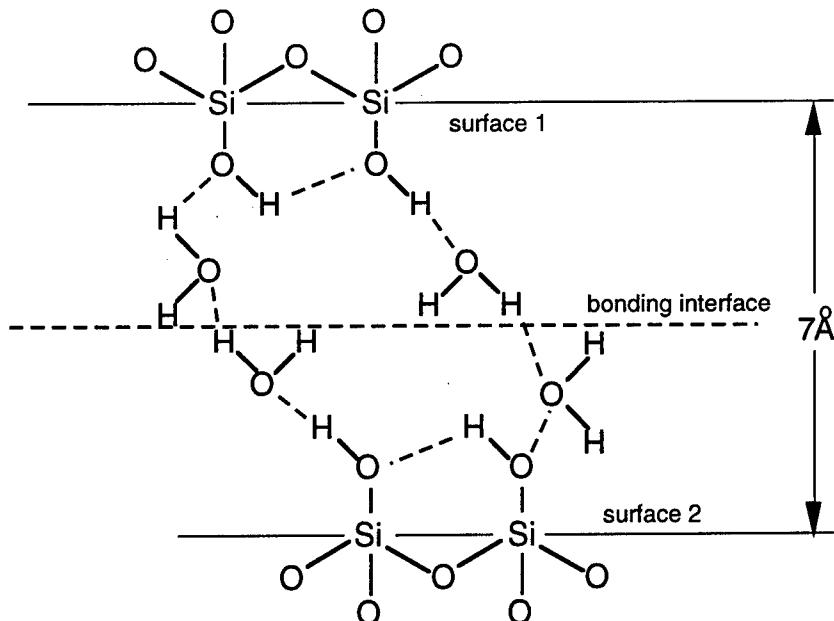
Initially, from room temperature (RT) to 110°C, mobile water at the interface of the two wafers can slowly convert any remaining Si-O-Si bonds on both surfaces into Si-OH bonds. This leads to a more OH groups available to form hydrogen bonds across the interface, see Figure 6.2. The process is represented in the following form:



Above 110°C, molecular water desorbs from the bond interface by polymerization of silanol (Si-OH) groups across the interface. Which is represented in the following form:



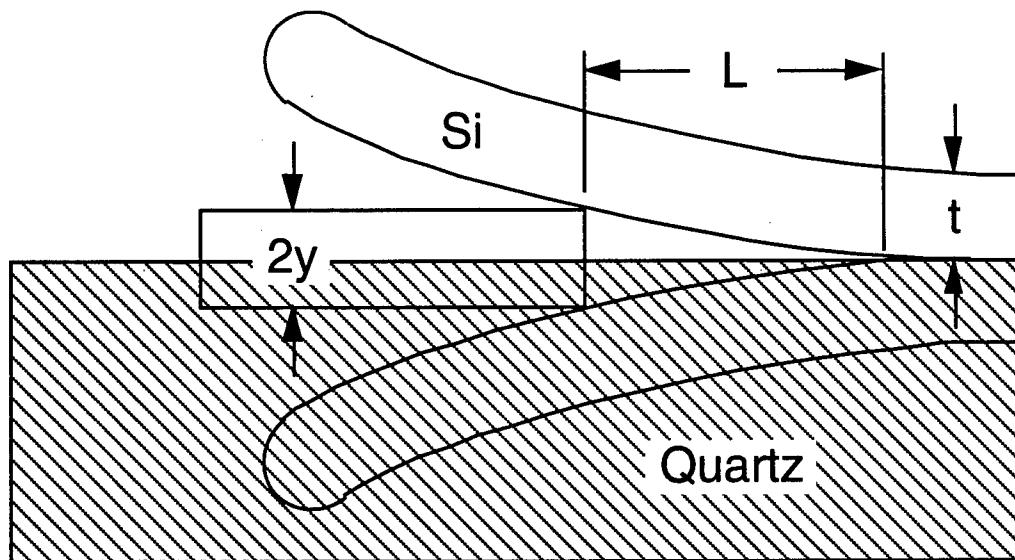
This implies that the silanol bonds, which are hydrogen bonded between opposite surfaces, should be transformed into strong siloxane (Si-O-Si) bonds. At approximately 150°C , almost all silanol groups are converted to siloxane bonds.



**Figure 6.2** Water bridging<sup>2</sup> between two hydrophilic Si wafers

### 6.3 Bond Strength Equation

The strength of a wafer bond can be measured by a simple process of inserting a razor of known thickness in-between the bonded surfaces, and observing the length of the crack that develops<sup>35</sup>, as illustrated in Figure 6.3 below. The figure depicts both the case of silicon bonded to silicon, or other similar material, and the case of silicon bonded to quartz/glass. In the first case of similar materials, it is assumed that both wafers bend outward from the force of the razor. Whereas in the second case of dissimilar materials, the assumption is that the glass material does not bend, indicated by the solid block shape, and the silicon wafer does all the bending. This assumption affects the calculation for bond strength as shown in Eq. 3 below for the asymmetrical case, and in Eq. 4 below for the symmetrical case.



**Figure 6.3.** Bond Strength Measurement

The equation for bond strength in the asymmetrical case is:

$$\gamma = \frac{3Et^3y^2}{(16L^4)} \text{ Eq. 3}$$

The equation for bond strength in the symmetrical case is:

$$\gamma = \frac{3Et^3y^2}{(8L^4)} \text{ Eq. 4}$$

where Young's modulus,  $E_{Si}=1.66 \times 10^{12}$  dyne/cm<sup>2</sup> and the razor blade has a thickness of  $2y$  in the symmetrical case, but only  $y$  in the asymmetrical case.

For our purpose of bonding silicon to glass, the dissimilar materials case<sup>30</sup> equation was used:

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4(E_1 t_{w1}^3 + E_2 t_{w2}^3)} \text{ Eq. 5}$$

For fused quartz,  $E_Q=7.6 \times 10^{11}$  dyne/cm<sup>2</sup>. The assumption that the quartz is larger and therefore more rigid than the silicon is not true for our case of using a

thin wafer of quartz along with a wafer of silicon of the same dimension. Hence, equation 5 is needed.

## **6.4 Bonding Results:**

This section documents the bonding result for various test cases, including silicon on silicon, silicon on optical glass, silicon on quartz , and finally, silicon on FOP. The first attempts at bonding used LE mask glass, which was cumbersome to work with due to its size and square shape. Quartz wafers were purchased along with a spinner for spin drying and cleaning the wafers. The spinner made a great difference in bond quality, yielding more bubble free wafer bonds. Finally, a quick attempt to bond FOP to silicon was made.

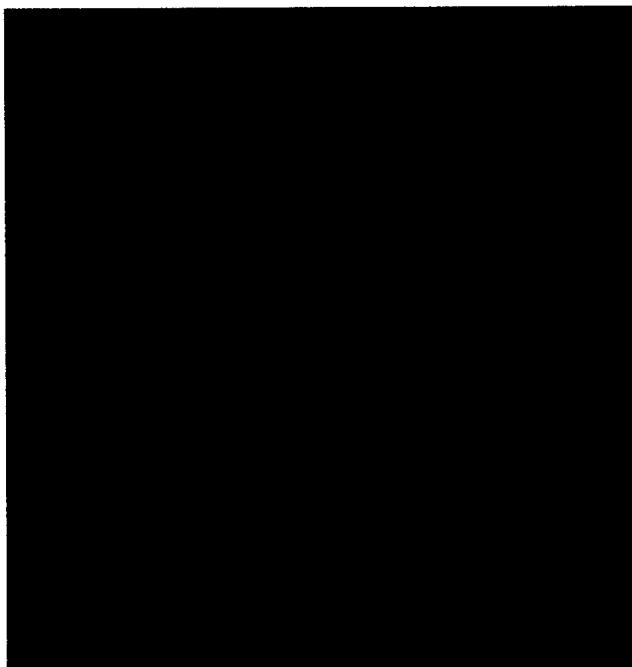
In all cases, the annealing process is critical for a good final bond. Due to the difference in thermal expansion of the silicon and glass, the temperature must be controlled precisely. The first oven used had poor temperature control so wafers debonded with big ( $>>1^{\circ}\text{ C}$ ) temperature swings. A second oven provided greater temperature control ( $<1^{\circ}\text{ C}$ ), and no debonding problems during the annealing process.

### **6.4.1 Si/Si Bonding:**

Two silicon wafer were bonded to test the bonding process. Initial bonds between silicon and glass yielded poor results, so this test served to answer the question of whether the cleaning process was at fault. The result illustrates the bonding that can be achieved. A good initial bond was obtained, indicating that the process was working. The indication seemed to be that the glass itself was the variable responsible for poor bonding. Note that this sample was annealed along with other Silicon/Glass samples so it baked for much longer than it needed to, which could also be a reason for the spots shown in Figure 6.5.



**Figure 6.4 Si/Si initial bond**



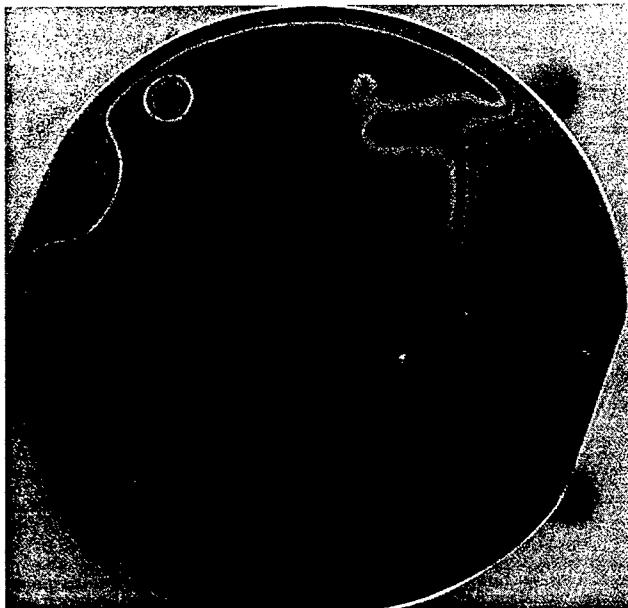
**Figure 6.5 Si/Si bond strength test**

The bond strength, from Figure 6.5, is 1303 dyne/cm. This is in good agreement with reported results<sup>29</sup>.

### **6.4.2 Si/Glass Mask Bonding:**

Figures 6.6 and 6.7 are two examples of early tests with silicon on Hoya glass. The composition of Hoya LE glass is: SiO<sub>2</sub>: 60%, B<sub>2</sub>O<sub>3</sub>: 5%, Al<sub>2</sub>O<sub>3</sub>: 15%, Na<sub>2</sub>O: 1%, K<sub>2</sub>O: 1%, RO: 18%. The thermal expansion coeff.  $3.7 \times 10^{-6}/^{\circ}\text{C}$ . Note that this is almost an order of magnitude greater than for quartz, which makes it expand faster (only slightly more) than silicon!

Difficulties in handling the large square plate of Hoya glass and the consequent exposure to contamination, are the main reasons for the poor bonding.



**Figure 6.6 Si/LE, first example**

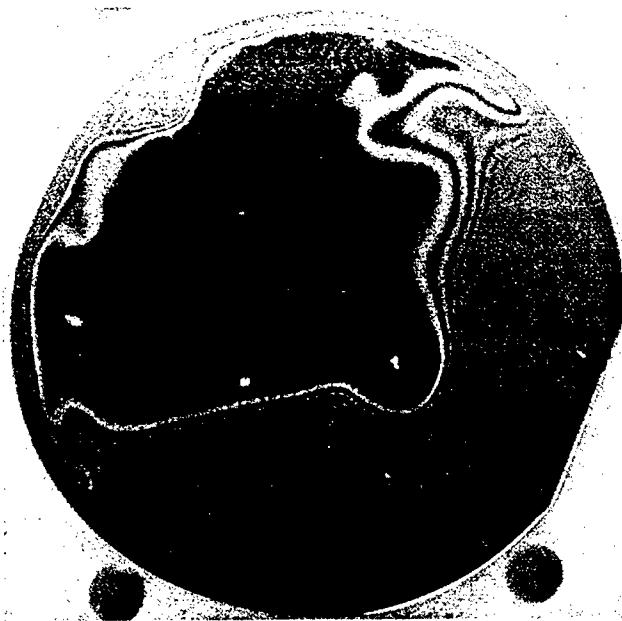
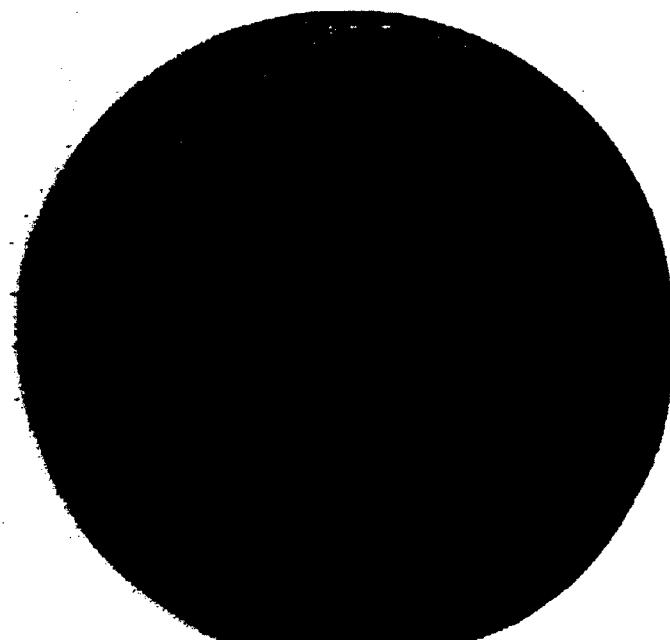


Figure 6.7 Si/LE, second example

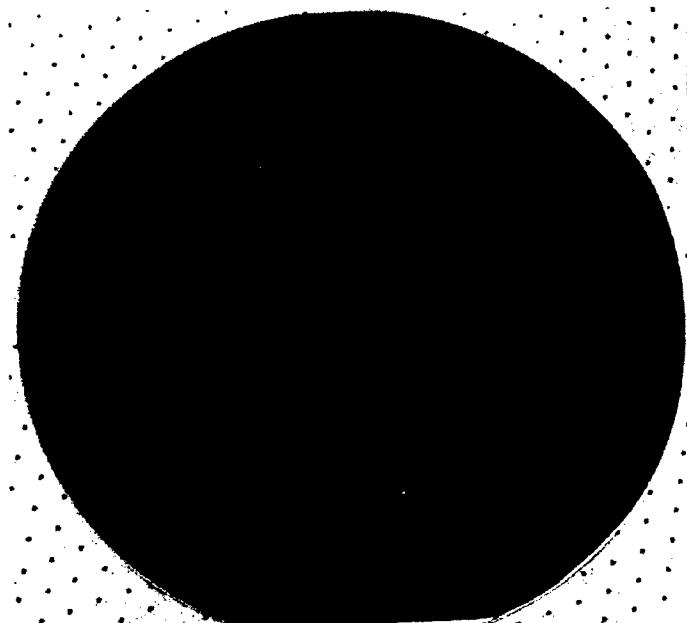
#### 6.4.3 Si/Quartz Bonding Using Ultra-pure H<sub>2</sub>O

Below are the first results of silicon to glass bonding where the spinner was used to clean and dry the wafers. The results were much improved over previous samples. Ultra pure water (Fisher Scientific Optima, Cat. No: W7-4) was used for the rinsing of the sample. Figure 6.8 shows the initial bonding, Figure 6.9 shows the bond after annealing, and Figure 6.10 shows results of the crack length test.

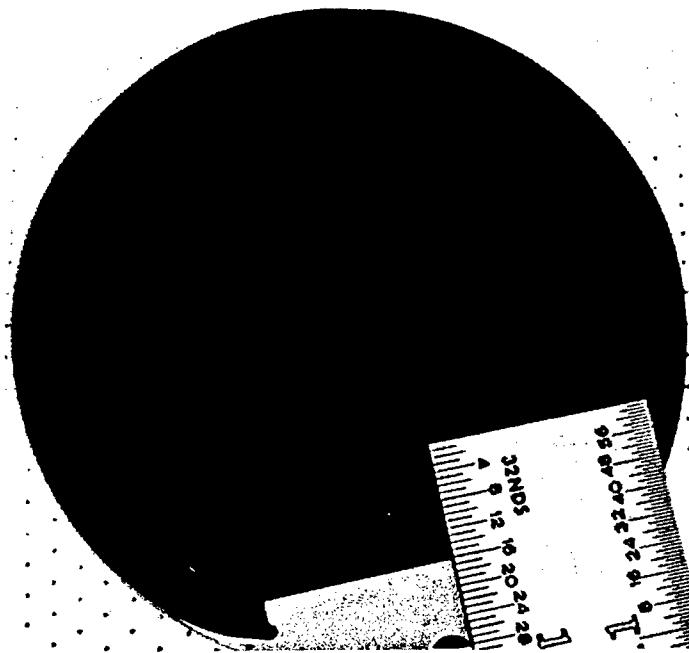
Note that this first run used the default factory settings of the spinner so the wafers did not dry well and needed to be spun twice. The cycle was: 20sec @ 500rpm, 20sec @ 1000rpm, 20sec @ 1500rpm, 20sec @ 2000rpm, 20sec @ 2200rpm, 20sec @ 500rpm, 20sec @ 100rpm. It has been suggested that the ultra-pure water helped with the low incidents of contamination, but the lack of drying was probably of greater benefit than the use of ultra-pure water. The sample in Figure 6.19-6.21, lends support to this notion since they too had water present during the initial bonding. The literature cited also support this theory<sup>29</sup>.



**Figure 6.8** Initial bond after using ultra-pure H<sub>2</sub>O

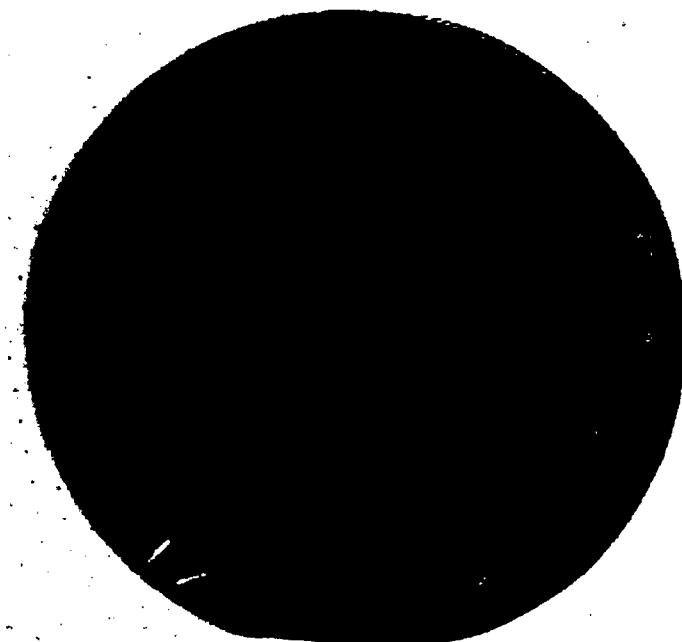


**Figure 6.9** Annealed bond after using ultra-pure H<sub>2</sub>O



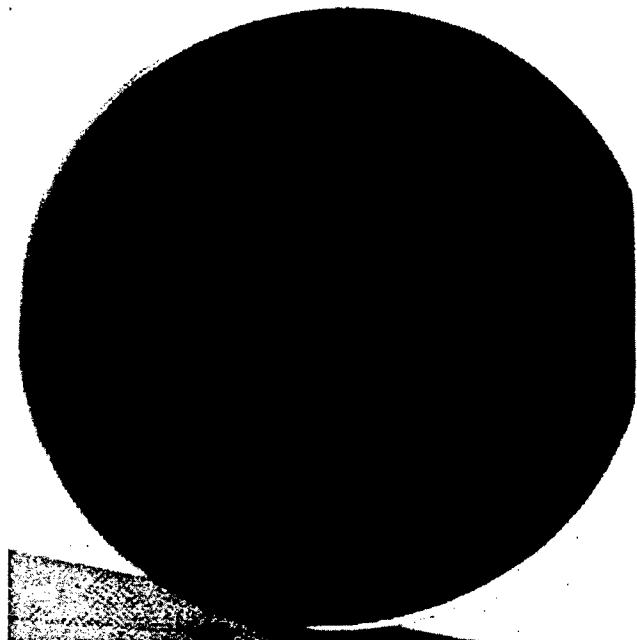
**Figure 6.10** Bond strength test of sample using ultra-pure H<sub>2</sub>O

The sample shown below in Figure 6.11 was blown with dry nitrogen while spinning to aid in the drying process, using the same spin times as above. This sample turned out to have more contamination presumably from the nitrogen blowing dirt in between the wafers. The nitrogen was not used again. The crack in the glass is the result of handling.

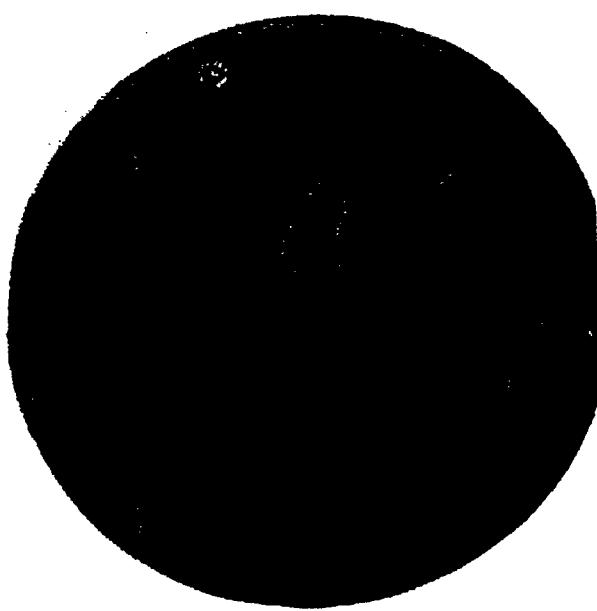


**Figure 6.11** Effects of Nitrogen blowing during spin drying

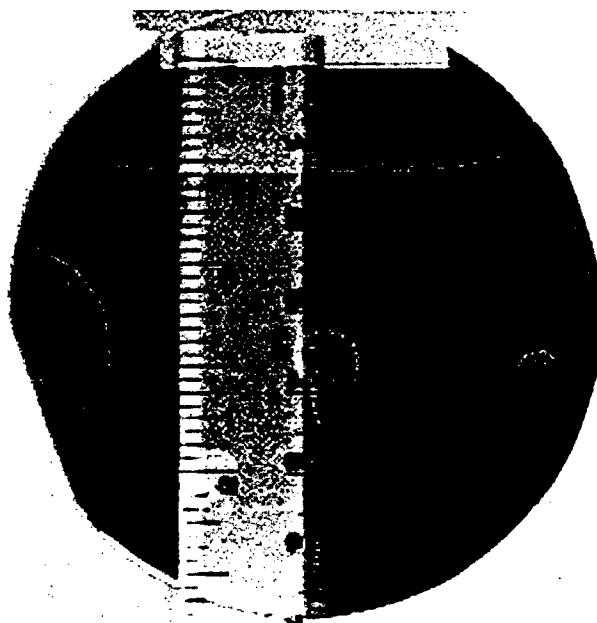
Figures 6.12-6.14 below are included to show bond results before the use of the spinner. This sample was dried on a hot plate at a low setting for about 20min. before bonding. The unbonded area near the edge is where the wafer was held with tweezers while bring the silicon into contact with the quartz wafer. Apparently, the tweezers affected the bonding at that edge.



**Figure 6.12 Initial bond, no spinner**



**Figure 6.13** Annealed bond, no spinner

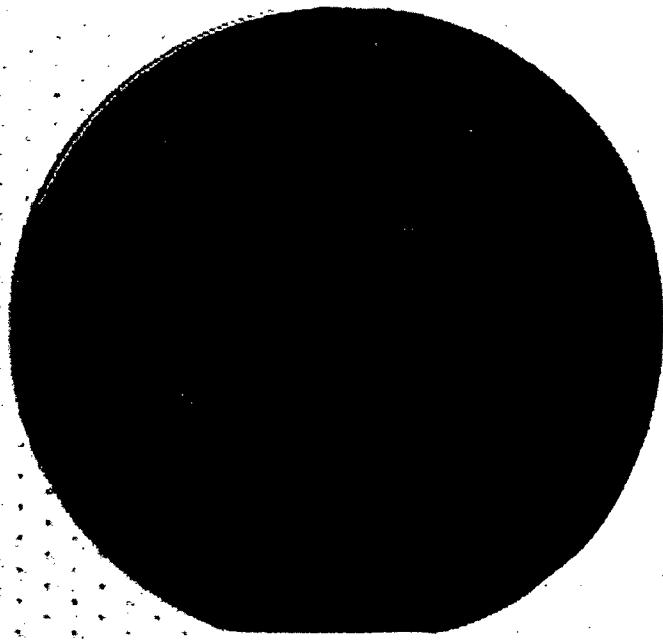


**Figure 6.14** Bond strength test, no spinner

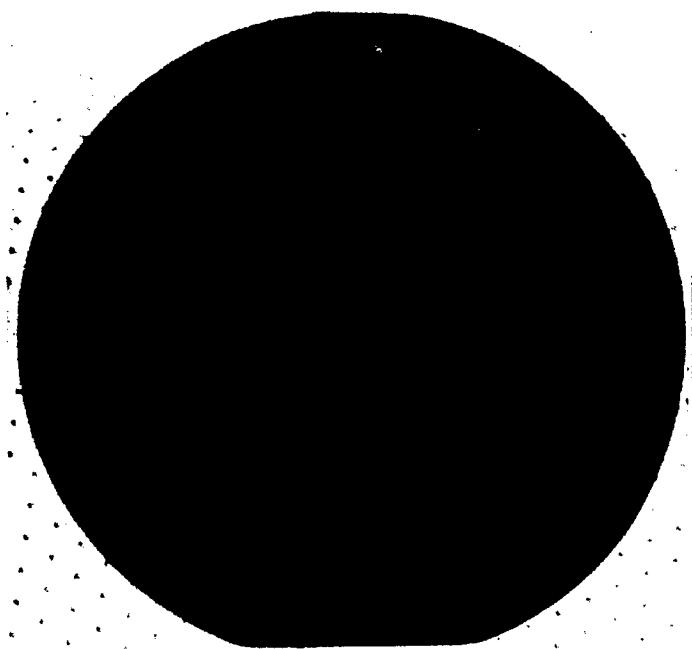
The bond strength, measured by Figure 6.14, was calculated to be 1269 dyne/cm.

#### **6.4.4 Si/Quartz Bonding With Use of Spinner:**

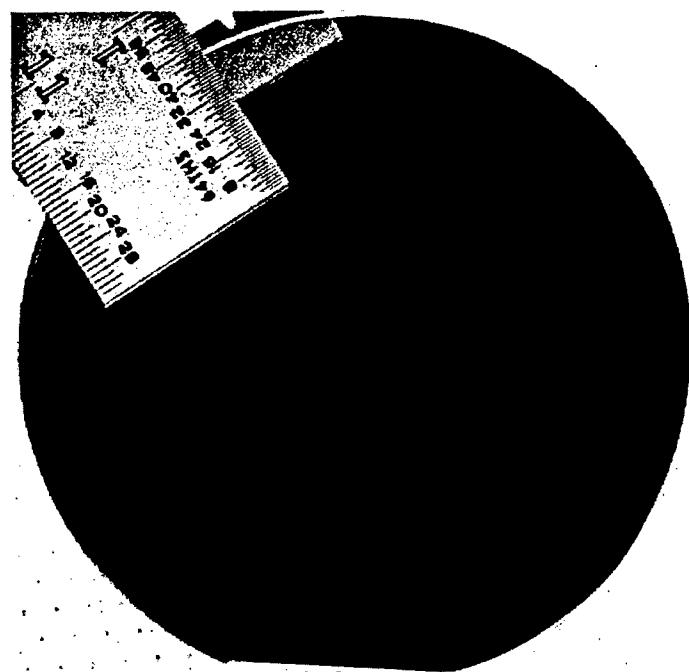
The following is an example of fairly clean bonding achieved with the use of the spinner. The spinner served two purposes. First the flushing action of the injected water followed by spinning helps to remove more contamination from the surfaces. Also, the design of the wafer chuck, following Tong and Gosele of Duke University<sup>35,36</sup>, allowed both wafers to be spun at once and bonded immediately after, thus minimizing the chances for further contamination. Again, Figure 6.16 shows the initial bonding, Figure 6.17 shows the bond after annealing, and Figure 6.18 shows results of the crack length test.



**Figure 6.15 Initial bond, with spinner**



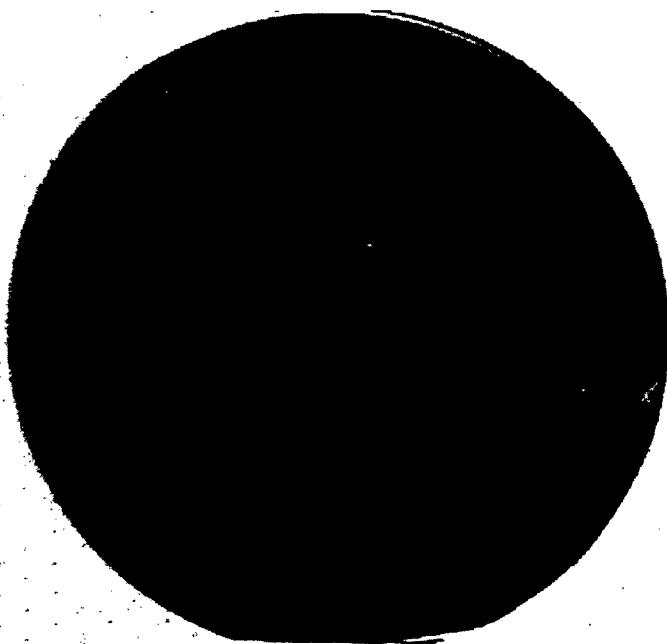
**Figure 6.16** Annealed bond, with spinner



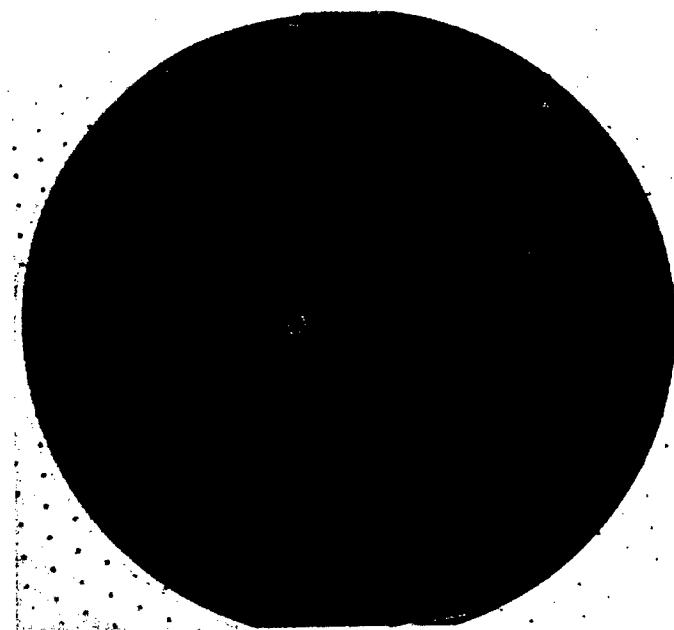
**Figure 6.17** Bond strength test, with spinner

#### **6.4.5 Effects of Relative Humidity on Bonding:**

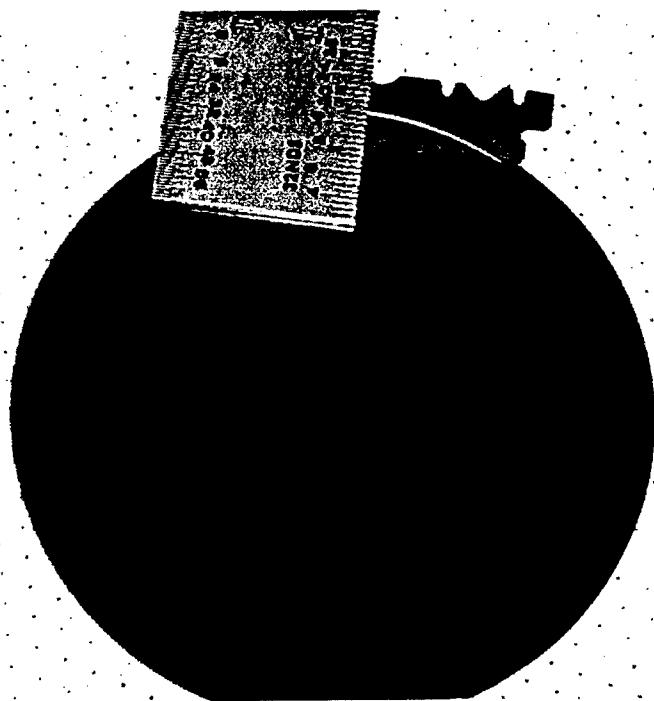
As noted in reference #29, page 1774, a relative humidity greater than 50% can aid in the bonding process. This was clearly seen with the sample below. A slight excess of water remained on the surface before the wafers were bonded. When the wafers were brought into contact, an obvious and fast contact wave was observed. In Figure 6.19, the excess water can be seen as swirls of gray lines. The annealing process successfully baked out the excess water to form a good bond, except for a few particles. As before, Figure 6.19 shows the initial bonding, Figure 6.20 shows the bond after annealing, and Figure 6.21 shows results of the crack length test.



**Figure 6.18 Initial bond, high humidity**



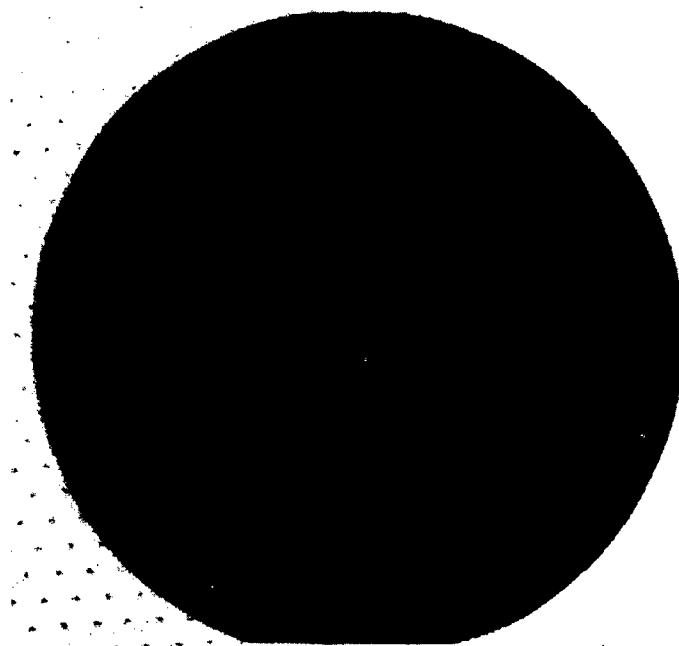
**Figure 6.19** Annealed bond, high humidity



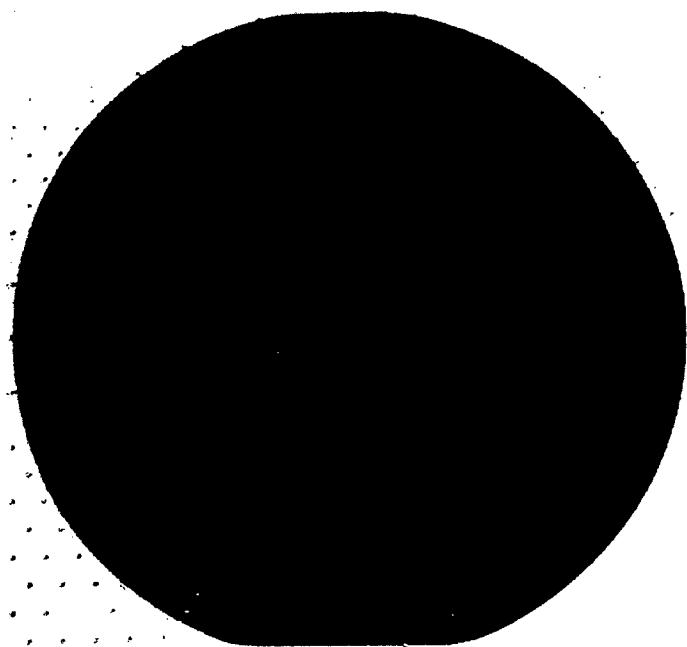
**Figure 6.20** Bond strength test, high humidity

#### **6.4.6 Effects of Annealing on Bonding:**

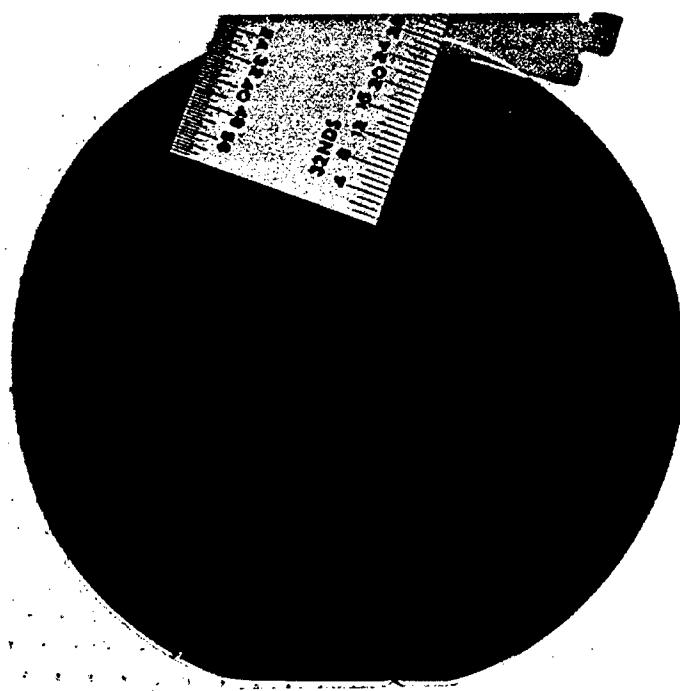
Note that the number of spots, in the following sample, decreases after annealing, and the ones that remain have fewer rings indicating that the wafers pulled in closer. This is most evident by the lower left spot changing from a light colored center to a dark center. Here again, Figure 6.22 shows the initial bonding, Figure 6.23 shows the bond after annealing with fewer spots, and Figure 6.24 shows results of the crack length test.



**Figure 6.21 Initial bond, many bubbles**



**Figure 6.22** Annealed bond showing fewer bubbles



**Figure 6.23** Bond strength test of reduced bubble sample

#### **6.4.7 Fiber Optic Plate Examples:**

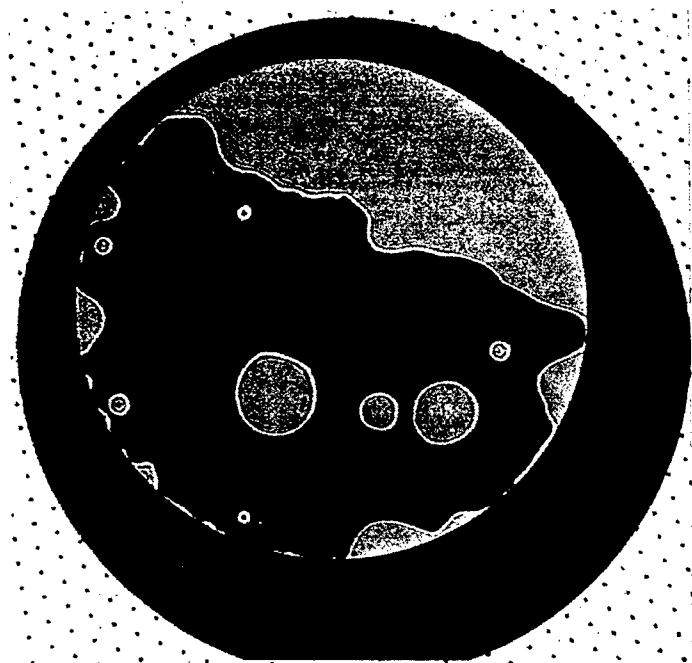
An attempt was made to bond FOP to SIMOX wafers. Since the Si wafers needed for the project were 100mm and the FOP's on hand were 75mm, only one wafer could be spun at one time. Available chucks could only handle 75mm or 100mm wafers. This led to the opportunity for more contamination, along with the general difficulty of handle the wafers while performing the initial bond. The method used was to drop the FOP's on the SIMOX wafer right after spinning the SIMOX wafer, and as soon as the lid of the spinner opened. Figure 6.25 and 6.26 show the results after annealing.

Sodium content is a concern in regards to the ability of the wafers to hydrophilic bond. It is known that traces of alkali ions can render the surface less hydrophilic by lowering the dehydroxylation temperature<sup>42</sup>. It has been demonstrated that the contact wave velocity is less for Si/Quartz than Si/Si most likely because of this reason<sup>29</sup>. Again, this fiber plate contains 13% Na in the core, and 7% Na in the cladding. The FOP has a coefficient of thermal expansion of  $8.9 \times 10^{-6}/^{\circ}\text{C}$ .



**Figure 6.24 First FOP on Silicon attempt**

The crack in the middle of Figure 6.25 is from excessive force used in testing the center bubble. Applying pressure indicated that the bubble contained trapped air.



**Figure 6.25** Second FOP on Silicon attempt

Even though only a small area is needed for this project, it is desirable to bond the two surfaces completely. The reason for this being that it has been reported that the etch used to thin the Si, also etches in the lateral direction at the bond interface at a fairly fast rate, as fast as 22-32 mm/h for KOH (potassium hydroxide) at 75° C. Etching with EDP (ethylendiamine pyrocatechol pyrazine) is an alternative which reportedly<sup>29,30</sup> has a lateral etch rate of 10-20% that of KOH.

## **6.5 Wafer Bonding Conclusion:**

Much of what has been reported involves the process of becoming familiar with hydrophilic wafer bonding and solving small, although non trivial, problems which stood in the way of good, clean wafer bonds. Control of contamination is a major factor and was initially the hardest to control, even in a cleanroom environment. A test case of bonding two silicon wafers yielded good results, indicating that at least the chemical cleaning process preformed well. The use of a spinner helped greatly by flushing remaining contamination away. The spinner design also allowed for immediately bonding after spinning, so as to not allow addition contamination on any surfaces. The use of ultra-pure water appears to be unnecessary.

Once the wafers were bonded, it became immediately evident that very stable temperature control of the annealing oven is critical for good bonding, or at least the prevention of debonding. Early samples suffered from debonding during large temperature swings in the manually controlled oven. The temperature stability needs to be at least within 1° C to prevent debonding.

The key factor for successful bonding appears to be the relative humidity of the environment the initial during wafer bonding. Samples which were bonded while still wet (a thin layer of water was still visible) bonded easily and exhibited bonding comparable to, or better than other samples which were bonded while completely dry. Actually, some samples that were dry had to be forced together to achieve bonding. Ideally, the wafers should be spun completely dry to remove contamination, and bonded in an environment which has a relative humidity of at least 50%, which would provide enough water to facilitate in the bonding process.

## **7. Conclusion:**

An optical interconnect scheme has been presented that overcomes the alignment and cost problems typically associated with this technology. The target computer systems for this scheme is a stacked multichip-module computer design as might be found in next generation aircraft, UAV, satellite, or missile system. This scheme is not reliant on costly micro-optical systems and does not require the expensive precision alignment typically required of complex optical interconnect schemes.

In the pursuit of a demonstration of this optical interconnect scheme, advances were made in the design and fabrication of photodetector and LED arrays and in wafer bonding. The concept of bonding a semiconductor wafer to a fiber optic plate wafer and then thinning the semiconductor wafer has powerful implications. Emitter and detector die can be produced which can be emit or detect from both the top and bottom of the die. Such functionality would simplify many optical interconnect schemes and would produce fast and efficient detectors.

The limitations of this scheme are the challenge of incorporating the optically guiding material into standard multichip-module packages and the poor thermal conductivity of the optically guiding material. The integration issue may be addressed by the 'chip first' MCM designs such as the General Electric High Density Interconnect (HDI). The 'chip first' module has the in-plane electronic interconnects applied on top of the module after the chips are in place giving some flexibility in choice of MCM substrate material. A new plastic HDI design would seem to allow for the embedding of the FOP material. The poor thermal conductivity of the FOP material requires that it be used only in those areas requiring optical interconnects or alignment marks. System designers will have to determine if the advantages of the higher throughput optical interconnects are worth the poor thermal conductivity penalty.

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